Exhibit 20

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

ACQIS LLC, a Texas limited liability company Plaintiff, v. MICROSOFT CORPORATION, a Washington corporation. Defendant.	§ § § § § § § § § §	Civil Action No. 6:22-cv-385-ADA **JURY TRIAL DEMANDED**
ACQIS LLC, a Texas limited liability company Plaintiff, v. SONY INTERACTIVE ENTERTAINMENT INC., a Japanese corporation, and SONY INTERACTIVE ENTERTAINMENT LLC, a California limited liability corporation. Defendants.	§ § § § § § § § § §	Civil Action No. 6:22-cv-386 **JURY TRIAL DEMANDED**

DECLARATION OF ANDREW WOLFE, PH.D

I, Andrew Wolfe, hereby declare the following:

I. INTRODUCTION

1. I submit this declaration as a technical expert in support of Sony Interactive Entertainment LLC, Sony Interactive Entertainment Inc., and Microsoft Corporation (collectively, "Defendants") in the above captioned case to provide my technical opinions regarding claim construction of patents asserted by ACQIS LLC ("ACQIS"), including U.S. Patent Nos.

9,529,768 ("the '768 patent"), 9,703,750 ("the '750 patent"), 8,977,797 ("the '797 patent"), RE 44,654 ("the '654 patent"), and RE 45,140 ("the '140 patent") (collectively, "ACQIS Asserted Patents").

2. I am being compensated at my standard hourly consulting rate. My compensation is not contingent on the outcome of the above-captioned case or on any claim construction ruling by the Court. Similarly, my compensation is not contingent on the substance of my opinions or the contents of my declaration. I do not have any financial interest in either of the parties in this case.

3. In reaching my opinions in this matter, in addition to materials specifically referenced herein, I have reviewed the following materials:

- U.S. Patent No. 9,529,768 to Chu ("'768 Patent");
- '768 Patent File History;
- U.S. Patent No. 9,703,750 to Chu ("'750 Patent");
- '750 Patent File History;
- U.S. Patent No. 8,977,797 to Chu ("'797 Patent");
- '797 Patent File History;
- U.S. Patent No. RE 44,654 to Chu ("'654 Patent");
- '654 Patent File History;
- U.S. Patent No. RE 45,140 to Chu ("'140 Patent");
- '140 Patent File History.

II. BACKGROUND AND QUALIFICATIONS

4. I have summarized in this section my educational background, career history, and other relevant qualifications. A current version of my curriculum vitae is attached as **Appendix A**.

5. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analysis to businesses on processor technology, computer systems, display technology, consumer electronics, software, design tools, data security, cryptography, and intellectual property issues. I have more than thirty years' experience

developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

6. In 1985, I earned a B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received a M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University. In 1992, I received a Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

7. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Touch Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for the Linus WriteTop, which many believe to be the first commercial tablet computer.

8. From 1986 through 1987, I designed and built a high-performance computer system at Carnegie Mellon University. From 1986 through 1988, I also developed the curriculum and supervised the teaching lab for the processor design courses.

9. In 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology

Division. I designed and built a bus interface and memory controller for a workstation-based computer system and worked on the design of a multiprocessor system.

10. At the end of 1989, along with some partners, I reacquired the technology I had developed at Touch Technology and at AMP and founded The Graphics Technology Company. As an officer and a consultant, I managed engineering development activities at that company and personally developed dozens of interactive graphics and interactive video computer systems over the next seven years.

11. I have consulted, formally and informally, for a number of processor design companies. In particular, I have served on the technical advisory boards for two media processor design companies, BOPS, Inc., where I chaired the board, and Siroyan Ltd. I served in a similar role for three networking chip companies, Intellon, Inc., Comsilica, Inc., and Entridia, Inc. and one 3D game accelerator company, Ageia, Inc. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director of Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for consumer gaming and related applications.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems courses, as well as conducting sponsored research in the area of computer systems and related topics. I also was a principal investigator for DOD research in video technology and a principal investigator for the New Jersey Center for Multimedia Research. From 1999 through 2002, I also taught the Computer Architecture course to both undergraduates and graduate students at Stanford University several times as a Consulting Professor. At Princeton, I

received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University, teaching courses on Microprocessor Systems, Real-time Embedded Systems, Advanced Digital Logic, and Mechatronics in the Electrical and Computer Engineering, Computer Science and Engineering, and Mechanical Engineering departments.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held PC graphics company originally called S3, Inc. and later called Sonicblue Inc. These included Chief Technology Officer, Vice President of Systems Integration Products, Senior Vice President of Business Development, and Director of Technology. At the time I joined S3, it supplied graphics accelerators for more than 50% of the PCs sold in the United States. In my roles at S3, I also supplied technology and components for 3D gaming to PC manufacturers and to platform developers such as Microsoft and Nintendo. As CTO, I managed the video research laboratory including the development of interface chips for laptops and other flat-panel displays. I also managed the development of three different laptop graphics chips incorporating LVDS technology. I led the development and introduction of more than 30 new consumer electronics products. I was also part of a team that developed the Frontpath Progear tablet computer in 2000.

14. I have published more than 50 peer-reviewed papers in computer architecture and computer systems design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design. I am a named inventor on at least fifty-six U.S. patents and thirty-seven foreign patents. I am a Fellow of the IEEE and a Distinguished Contributor to the IEEE Computer Society.

15. I have been the invited keynote speaker at the ACM/IEEE International Symposium

on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events, including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show, as well as at the Harvard Business School and the University of Illinois Law School. I have been interviewed on subjects related to computer graphics and video technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune, as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice, and Duke.

16. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my CV.

17. In summary, I have extensive familiarity with computer architectures, signaling methodologies, processors, busses, and graphics, among other computer technologies. Counsel has asked me to assume that the claimed priority date of the ACQIS Asserted Patents is May 14, 1999 for the '654 and '140 Patents and May 12, 2000 for the '768, '750 and '797 Patents ("the time of the invention"), which I understand is what ACQIS has contended. I am familiar with what the state of art was at each of these times.

III. LEGAL FRAMEWORK

18. I am a technical expert and do not offer any legal opinions. However, counsel has informed me that the claim construction process is governed by a number of legal principles, and I have used them in rendering my opinions.

19. I understand that patent claim terms are given their plain and ordinary meaning as

would be understood by a person having ordinary skill in the art at the time of the invention in light of the claim language itself, the patent specification, and the prosecution history.

20. I understand that a person having ordinary skill in the art is a fictional, objective person who has the average knowledge, skill, and expertise in the claimed invention's technical or scientific field.

21. I understand that a patent is invalid under the doctrine of indefiniteness if its claims, read in light of the patent's specification and prosecution history, fail to inform with reasonable certainty persons skilled in the art about the scope of the invention. I understand that a consideration of whether a patent's claim is indefinite must take into account the inherent limitations of language, but that a patent's claim nevertheless must be precise enough to provide reasonably clear notice of what is claimed so that members of the public understand what is still open to them. I understand that when a term of degree is used in a claim the patent must provide some standard for measuring that degree. I further understand that when a subjective term is used in a claim the patent must provide some standard for measuring the scope of the term that provides objective boundaries for those skilled in the art.

IV. LEVEL OF ORDINARY SKILL IN THE ART

22. I understand that the '797 Patent was filed on October 10, 2012 as a continuations of a series of patents, the first of which was filed on May 12, 2000. I also understand that the '768 and '750 Patents are continuations of the '797 Patent and share the same specification. I also understand that these patents claim priority to a provisional application filed on May 14, 1999. I understand that the two reissued Asserted Patents (the '654 and '140 patents) both trace back to a patent application filed on May 14, 1999. '654 patent at (64); ('140 patent) at (64). At this time, I have not been asked to determine whether the claims of ACQIS's Asserted Patents are

supported by any application to which it claims priority. However, my opinions herein are the same regardless of which date is used, May 14, 1999 or May 12, 2000.

23. In determining the characteristics of a person having ordinary skill in the art ("POSITA") of ACQIS's Asserted Patents at the time of the claimed invention, I considered several factors, including the type of problems encountered in the art, the solutions to those problems, the rapidity with which innovations are made in the field, the sophistication of the technology, and the education level of active workers in the field. I also placed myself back in the time frame of the claimed invention and considered the colleagues with whom I had worked at the time.

24. In my opinion, the level of skill of a POSITA is a person who had at least a Master's Degree in electrical engineering, computer science, or a related subject, or a Bachelor's Degree in electrical engineering, computer science, or a related subject and three years of experience working with computer architecture, computer buses, and related technologies. I understand that ACQIS has used the following definition for the level of ordinary skill in past proceedings: "[A] person of ordinary skill in the art ("POSITA") concerning the technology described and claimed in the ACQIS patents-in-suit would have at least a bachelor's degree or the equivalent in computer or electrical engineering (or related academic fields) and three to four years of additional experience in the field of computer architecture, computer system design, or computer communication protocols, or a closely related area of endeavor, or an equivalent combination of education and experience." My opinions are the same under either level of skill of a POSITA.

25. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a person having ordinary skill in the art at the time of the invention. Additionally, I was at least a person having ordinary skill in the art as of May 14, 1999, at latest.

V. OPINION

A. "low voltage differential signal [channel]" / "LVDS [channel]"

26. I understand that each of the Asserted Claims of the ACQIS Asserted Patents either directly or indirectly recite the term "low voltage differential signal (LVDS) channel" or "LVDS channel." Exemplary claim limitations using LVDS are reproduced below:

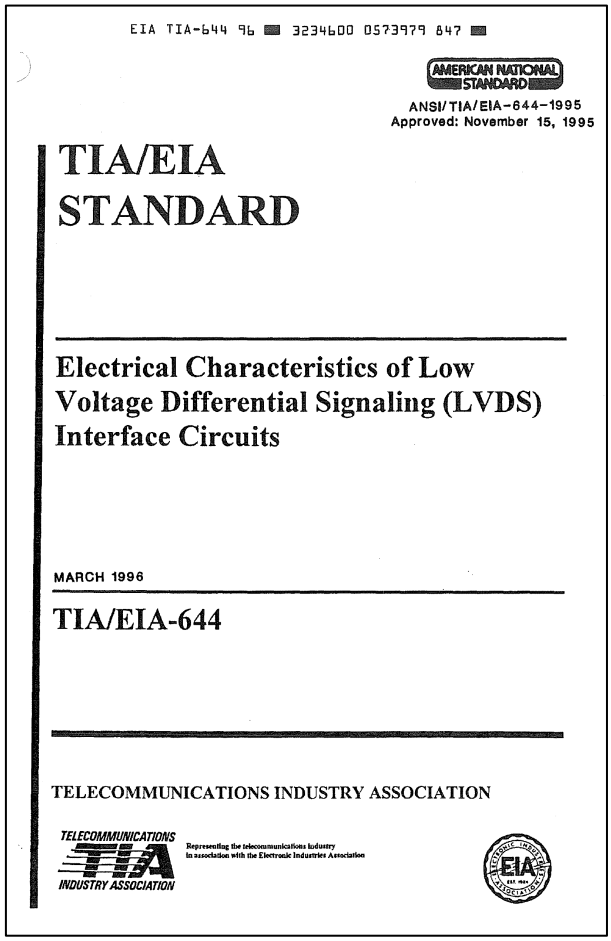
Claim	Limitation
'750 Patent, Claim 1	a first ***Low Voltage Differential Signal (LVDS) channel*** directly extending from the interface controller to convey address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial bit stream, wherein the first ***LVDS channel*** comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction;
'750 Patent, Claim 5	an integrated central processing unit and graphics subsystem in a single chip directly connected to a first ***Low Voltage Differential Signal (LVDS) channel*** to convey encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in serial form, wherein the first ***LVDS channel*** comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction
'750 Patent, Claim 24	a second ***LVDS channel*** coupled to the connector, adapted to convey Universal Serial Bus (USB) protocol data packets, wherein the second LVDS channel comprises two unidirectional, differential signal pairs that transmit data packets in opposite directions; and
'768 Patent, Claim 1	a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction;
'797 Patent, Claim 33	conveying a ***first Low Voltage Differential Signal (LVDS) channel*** through the connector comprising two unidirectional, serial channels that transmit data in opposite directions; conveying Universal Serial Bus (USB) protocol data from the integrated CPU and graphics controller chip, over the first ***LVDS channel*** for external USB protocol data communication

'140 Patent, Claim 14	providing a first ***Low Voltage Differential Signal (LVDS) channel*** to couple to the connector, the first ***LVDS channel*** comprising two unidirectional, serial bit channels that transmit data in opposite directions
'654 Patent, Claim 20	connecting a first ***Low Voltage Differential Signal (LVDS) channel*** directly to said integrated CPU and graphics controller, the first ***LVDS channel*** comprising two unidirectional, serial channels that transmit data in opposite directions; *** providing a second ***LVDS channel*** to couple to the console through the connector, the second ***LVDS channel*** comprising two unidirectional, serial channels that transmit data in opposite directions; and enabling Universal Serial Bus (USB) protocol data to be conveyed over the second ***LVDS channel***.

27. As discussed above, it is my understanding that ACQIS contends that the Asserted Patents have a priority date, at earliest, of May 14, 1999. As of this date, the acronym LVDS, which stood for low voltage differential signaling, was a well-known technology to a POSITA. For example, I met with Dave Gustavson and David James of the SCI standards team around 1995 when they were touring universities promoting the "LVDS" technology in that standard. I also managed teams that developed and tested "LVDS" technology in chips and video cards beginning in 1997 through 2000.

28. A POSITA would have understood that LVDS was defined in two relevant industry standards:

- **ANSI/TIA/EIA-644**, "TIA/EIA Standard, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits," Telecommunications Industry Association (approved November 15, 1995), attached hereto as **Appendix B**.



EIA TIA-644 96 ■ 3234600 0573979 847 ■

AMERICAN NATIONAL STANDARD

ANSI/TIA/EIA-644-1995
Approved: November 15, 1995

TIA/EIA
STANDARD

Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

MARCH 1996

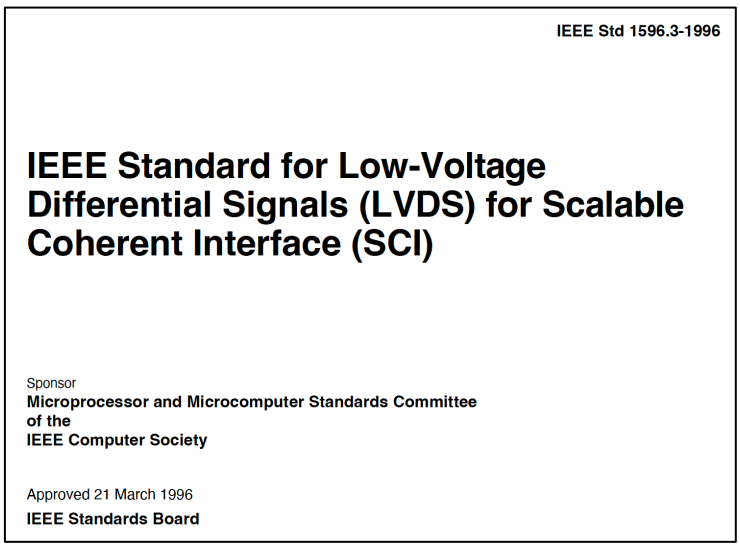
TIA/EIA-644

TELECOMMUNICATIONS INDUSTRY ASSOCIATION

TELECOMMUNICATIONS TIA INDUSTRY ASSOCIATION
Representing the telecommunications industry in association with the Electronic Industries Association

EIA

- **IEEE 1596.3**, "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)," Institute of Electrical and Electronics Engineers, Inc. Standards Board (approved March 21, 1996), attached hereto as **Appendix C**.



IEEE Std 1596.3-1996

IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

Sponsor
Microprocessor and Microcomputer Standards Committee of the IEEE Computer Society

Approved 21 March 1996
IEEE Standards Board

29. Consistent with this understanding, the '750 and '768 Patents specifically reference the ANSI/TIA/EIA-644 Standard. '750 patent at Page 6 (References Cited) and '768 patent at Page 6 (References Cited) (identifying "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, TIA/EIA Standard, TIA/EIA-644, Mar. 1996, 42 pages"). The ANSI/TIA/EIA-644 Standard, in turn, specifically identifies IEEE 1596.3 as another "standard." ANSI/TIA/EIA-644 Standard at p. v, Foreword.

30. The Asserted Patents describe the same benefits of using LVDS as those found in the ANSI/TIA/EIA-644 LVDS Standard.

ANSI/TIA/EIA-644 LVDS Standard	'750 Patent
"The voltage levels specified in this Standard were specified such that maximum flexibility would be provided, while providing a low power, high speed, differential interface. … The low voltage (330 mV) swing limits power dissipation, while also reducing radiation of EMI signals." ANSI/TIA/EIA-644 at p. v (Foreword).	"It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel." '750 Patent at 4:11-16.

31. The '750 and '768 Patents cite to additional documents supporting the fact that a

POSITA would have understood that LVDS refers to the technology described in ANSI/TIA/EIA-644 or IEEE 1596.3. In the "LVDS Owner's Manual," National Semiconductor – a well-known semiconductor manufacturer – stated that "two key industry standards define LVDS."

> **1.2.3 The LVDS Standards**
>
> Two key industry standards define LVDS: one from the ANSI/TIA/EIA (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) and another from the IEEE (Institute for Electrical and Electronics Engineering).

Appendix D, "National Semiconductor LVDS Owner's Manual" (1st Edition, Spring 1997), at 2. This document is cited by the '750 Patent at Page 9 of the "References Cited" and by the ''768 Patent at Page 9 of the "References Cited."

32. These "two key industry standards" are ANSI/TIA/EIA-644 and IEEE 1596.3.

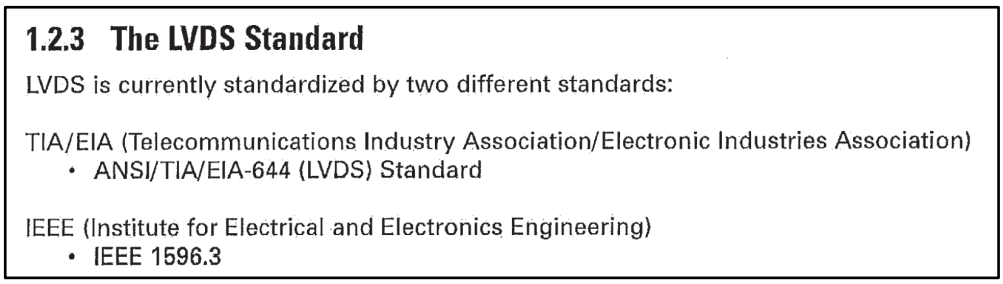
> The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

> The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

> The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the **IEEE 1596.3** standard. SCI-LVDS specifies also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

Appendix D, "National Semiconductor LVDS Owner's Manual" (1st Edition, Spring 1997), at 2-3.

33. A subsequent edition of the "LVDS Owner's Manual" similarly defined LVDS as being "standardized" by the "ANSI/TIA/EIA-644 Standard" and "IEEE 1596.3."



1.2.3 The LVDS Standard

LVDS is currently standardized by two different standards:

TIA/EIA (Telecommunications Industry Association/Electronic Industries Association)
- ANSI/TIA/EIA-644 (LVDS) Standard

IEEE (Institute for Electrical and Electronics Engineering)
- IEEE 1596.3

Appendix E, "National Semiconductor LVDS Owner's Manual" (2nd Edition, Spring 2000), at 1. This document is cited by the '750 Patent at Page 12 of the "References Cited" and by the ''768 Patent at Page 12 of the "References Cited."

34. Similarly, "An Overview of LVDS Technology" defines LVDS by the same two standards: "There are two industry standards that define LVDS. The more common of the two is the generic electrical layer standard defined by the TIA. This standard is known as ANSI/TIA/EIA-644. The other application specific standard is an IEEE … standard titled Scalable Coherent Interface (SCI)." **Appendix F**, Huq, S., et al., "An Overview of LVDS Technology," Application Note 971 (Jul. 1998) at p. 1. This document is cited by '750 patent at Page 6 of the "References Cited" and '768 patent at Page 6 of the "References Cited."

35. Additional documents define LVDS in a similar manner. In answering the question "What is LVDS?," Pericom stated "LVDS is defined in the TIA/EIA-644 standards and the IEEE 1596.3 standards." **Appendix G**, Ma, J., "A Closer Look at LVDS Technology," Application Note 41 at 1 (Pericom Nov. 16, 2001).

36. Further, a POSITA would have understood that the use of the known, capitalized acronym, "LVDS," was meant to refer to a specific technology, as defined by the standards discussed above.

37. In view of the foregoing, as of the priority dates of the Asserted Patents, a POSITA would have understood that the phrase "low voltage differential signal (LVDS) channel" or

"LVDS channel" to mean "a channel for carrying a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3."

38. Without the context of the standards, the phrase "low voltage differential signal," and associated acronym "LVDS," become a subjective determination if there is no corresponding requirement tying LVDS to one of the "key industry standards" that define LVDS. For example, there is no context as to what constitutes a "low voltage differential signal." Thus, objective criteria are necessary to assess what qualifies as a "low voltage differential signal" as compared to a signal that is not a "low voltage differential signal" in the context of the Asserted Patents, which also includes claims reciting generic "differential signals." The plain language of the claims merely requires that a "low voltage differential signal" be provided or used to convey certain types of data" but there are no objective criteria in the claims themselves that provide any insight to a person having ordinary skill in the art regarding the boundaries of these subjective terms.

39. As explained above, I understand that when a term of degree or a subjective term is used in a patent claim, the specification must provide a standard for measuring the scope of the term such that a person having ordinary skill in the art would understand the objective boundaries of the claim.

40. I have analyzed the specifications of ACQIS's Asserted Patents[1], and I have found no standard that would allow a person of ordinary skill to understand the objective boundaries of what qualifies as a "low voltage differential signal." Indeed, the disclosures regarding "low voltage differential signal" from the specifications of ACQIS's Asserted Patents (exemplary disclosures reproduced below) generally describe LVDS, but do not describe any standards or criteria for

[1] I note that I also analyzed the file histories of the Asserted Patents. However, the term "low voltage differential signal [channel]" or "LVDS [channel]" was not substantively discussed.

differentiating a "low voltage differential signal" from the voltages of other differential signals.

> It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

'750 Patent at 4:11-18.

> This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses.

'750 Patent at 5:65-6:5.

> FIG. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC.

'750 Patent at 22:41-44.

> FIG. 31 is a schematic diagram of the lines PCK and PD0 to PD3. These lines are unidirectional LVDS lines for transmitting signals from HIC 2900 to PIC 3000. Another set of lines, namely PCKR and PDR0 to PDR3, are used to transmit clock signals and bits from PIC 3000 to HIC-2900.

'750 Patent at 24:26-30.

> For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.
>
> The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

'750 Patent at 24:41-50.

> For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.
>
> A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

'750 Patent at 24:65-25:5.

> Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

'750 Patent at 26:58-61.

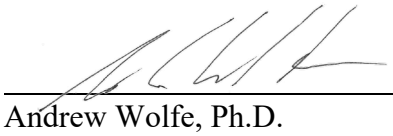
41. As can be seen from the above, the ACQIS Asserted Patents do not provide any guidance on how a person of ordinary skill in the art would determine whether a given signal or channel is a "low voltage differential signal."

42. Without this guidance, the scope of the claims are unknown to a POSITA because "low" is a term of degree and subjective. What is "low" and what is not "low" is completely unknown with no objective baseline against which "low" can be measured.

43. For these reasons, a person of ordinary skill in the art ***would not*** understand the scope of the term "low voltage differential signal" with any reasonable certainty unless it is defined in the context of the well-known standards defining the same. Therefore, in my opinion, this term is indefinite unless it is construed "in accordance with" the relevant standards at the time of the invention.

44. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: May 18, 2023



Andrew Wolfe, Ph.D.

APPENDIX A

Andrew Wolfe Ph.D.

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(408) 394-1096 (mobile)
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Education:

Ph.D. in Computer Engineering, Carnegie Mellon University, 1992
Visiting Graduate Student, Center for Reliable Computing, Stanford University, 1988-1989
M.S. in Electrical and Computer Engineering, Carnegie Mellon University, 1987
B.S.E.E. in Electrical Engineering and Computer Science, The Johns Hopkins University, 1985

Recent Employment:

Lecturer, [September 2013-present]
Santa Clara University

Teaching graduate and undergraduate courses on embedded computing, mechatronics, real-time systems, computer architecture, and community service.

Consultant, [October 2002-present]
Wolfe Consulting

Consultant on processor technology, computer systems, consumer electronics, software, design tools, and intellectual property issues. Testifying and consulting expert for IP and other technology-related litigation matters.

Sample clients include:

AMD	Nvidia	Samsung
IBM	Motorola/Lenovo	HTC
AT&T	Verizon Mobile	Huawei
Apple	T-Mobile	Western Digital
Nintendo	Google	Sonos
Sony	Netflix	Roku
Synaptics	Activision	Sawstop
Tivo	LG	TCL
Medigus	William Hill	ZTE
Egnyte	Acer	Waymo

Chief Technical Officer, [1999-2002]; Sr. VP of Business Development, [2001-2002]; VP, Systems Integration, S3 Fellow , [1998 – 1999]; Director of Technology, S3 Fellow , [1997 - 1998]
SONIC|blue, Inc, Santa Clara, CA (formerly S3 Inc.)

Strategic Business Development:
Developed and implemented strategy to reposition S3 from PC graphics into the leading networked consumer electronics company.

- Acquired Diamond Multimedia and coordinated integration of communications, Rio digital music, and workstation graphics divisions into S3.
- Identified and negotiated acquisitions to grow digital media businesses including Empeg, ReplayTV, and Sensory Science.
- Identified and negotiated strategic investments including Comsilica, Intellon, KBGear Interactive, Entridia, DataPlay and others.

- Developed strategy for integrated graphics/core-logic products and established a joint venture with Via Technologies to design and market these products.
- Negotiated divestiture of graphics chip business to Via and the workstation graphics division to ATI.

Product Planning and Development:

- Drove roadmap development within SONICblue product divisions.
- Managed Business Development for all product lines.
- Led New Product Development and Corporate Vision processes.
- Acting co-General Manager of Rio digital music business in 2nd half of 2001. Responsible for all areas of product development, business development, and cost management.
- Managed development of the Savage/MX and Savage/IX mobile 3D graphics accelerators and Savage/NB system logic products.

Public Relations, Public Policy and Investor Relations:

- Present company products and strategy at industry events such as CES, Comdex, and Microprocessor Forum.
- Discuss new products and initiatives with the press.
- Promote issues of interest to SONICblue to industry groups and in Washington.
- Brief analysts, and investors on company progress. Participate in quarterly conference calls.

IP Management and Licensing:

- Negotiated and managed partnership agreements including a critical cross-licensing agreement with Intel.
- Renegotiated technology-licensing agreements with IBM for workstation graphics products.
- Evaluated outside technology opportunities, managed video research and development, and managed corporate IP strategy with legal staff including patent filings, cross licensing, and litigation.

Consulting Professor , [1999-2002]
Stanford University, Stanford, CA

Teaching computer architecture and microprocessor design.

Assistant Professor [1991 - 1997]
Princeton University, Princeton, NJ

Teaching and research in the Electrical Engineering department. Research in embedded computing systems, multimedia, video signal processors, compiler optimization, and high performance computer architecture. Principal investigator or project manager for ~$6M in funded research.

Visiting Assistant Professor , [1992]
Carnegie Mellon University, Pittsburgh, PA

Research and preparation of teaching materials on advanced microprocessor designs including new superscalar and superpipelined processor architectures.

Founder and Vice President and Consultant, [1989 - 1995]
The Graphics Technology Company, Inc., Austin, TX

Founded company to develop touch-sensitive components and systems for the first generation of PDA devices and interactive public systems. Obtained financing from Gunze Corp., Osaka, Japan. Company is now part of 3M.

Senior Electrical Engineer, [1989]
ESL - TRW, Advanced Technology Division, Sunnyvale, CA

Designed the architecture for an Intel i860-based multiple-processor digital signal processing system for advanced military applications. Designed several FPGA interface chips for VME-bus systems.

Design Consultant, [1986 -1987]
Carroll Touch Division, AMP Inc., Round Rock, TX

Developed several new technologies for touch-screen systems. Designed the first ASIC produced for AMP, a mixed-signal interface chip for controlling touch-screen sensors. Developed the system electronics, system firmware, and customer utility software for numerous products including those based on the new ASIC.

Senior Design Engineer, [1983 -1985]
Touch Technology Inc., Annapolis, MD

Advisory Boards:

Director, Turtle Beach Corporation (NASDAQ:HEAR) (formerly Parametric Sound Corporation), KBGear Interactive, Inc., Comsilica, Inc., Rioport.com, various S3 subsidiaries.

Technical Advisory Boards, Ageia, Inc., Intellon, Inc., Comsilica, Inc., Entridia, Inc., Siroyan, Ltd., BOPS, Inc, Quester Venture Funds

Carnegie Mellon University Silicon Valley Advisory Board; Johns Hopkins University Tech Transfer Advisory Board

Awards:

IEEE Fellow - for contributions in hardware code compression of embedded software, power consumption analysis, and optimization, 2022
IEEE Computer Society Distinguished Contributor - 2021
Micro Test-of-Time Award (in recognition of one of the ten most influential papers of the first 25 years of the symposium), 2014
Business 2.0 "20 Young Executives You Need to Know", 2002
Walter C. Johnson Prize for Teaching Excellence, 1997.
Princeton University Engineering Council Excellence in Teaching Award, Spring 1996
AT&T/Lucent Foundation Research Award, 1996.
Walter C. Johnson Prize for Teaching Excellence, 1995
IEEE Certificate of Appreciation, 1995, 2001.
AT&T Foundation Research Award, 1993.
Semiconductor Research Corporation Fellow, 1986 - 1991.
Burroughs Corporation Fellowship in Engineering, 1985 - 1986.

Professional Activities:

Program Chair: Micro-24, 1991, Hot Chips 13, 2001.

General Chair: Micro-26, 1993, Micro-33, 2000.

Associate Editor: IEEE Computer Architecture Letters; ACM Transactions in Embedded Computing Systems

Speaker at CES, WinHec, Comdex, Intel Dev. Forum, Digital Media Summit, Microprocessor Forum, etc.

Keynote speaker at Micro-34, ICME 2002

IEEE B. Ramakrishna Rau Award committee – 2012-2016

IEEE Computer Society Awards Committee – 2015

CES Awards Judge – 2016

Entrepreneurship Mentor – Draper University

Over 50 refereed publications.

Publications since January 2006:

Wolfe, A., "Retrospective on Code Compression and a Fresh Approach to Embedded Systems", IEEE MICRO, July/Aug. 2016, Invited paper.

Patents:

U.S. Pat. 5,041,701 – *Edge Linearization Device for a Contact Input System*, Aug. 20, 1991.
U.S. Pat. 5,438,168 – *Touch Panel*, Aug. 1, 1995.
U.S. Pat. 5,736,688 – *Curvilinear Linearization Device for Touch Systems*, Apr. 7, 1998.
U.S. Pat. 6,037,930 – *Multimodal touch sensitive peripheral device*, March 14, 2000.
U.S. Pat. 6,408,421 – *High-speed asynchronous decoder circuit for variable-length coded data*, June 18, 2002.
U.S. Pat. 6,865,668 – *Variable-length, high-speed, asynchronous decoder circuit*, March 8, 2005
U.S. Pat. 7,079,133 – *Superscalar 3D Graphics Engine*, July 18, 2006
EP 1 661 131 B1 – *PORTABLE ENTERTAINMENT APPARATUS*, Jan. 21, 2009
U.S. Pat. 7,555,006 – *Method and system for adaptive transcoding and transrating in a video network*, June 30, 2009
U.S. Pat. 7,996,595 – *Interrupt Arbitration for Multiprocessors*, Aug. 9, 2011
EP 2 241 979 B1 – *Interrupt Arbitration for Multiprocessors*, Oct. 10, 2011
U.S. Pat. 8,131,970 – *Compiler Based Cache Allocation*, March 6, 2012
U.S. Pat. 8,180,963 – *Hierarchical read-combining local memories*, May 15, 2012
U.S. Pat. 8,193,941 – *Snoring Treatment*, June 5, 2012
U.S. Pat. 8,203,541 – *OLED display and sensor*, June 19, 2012
U.S. Pat. 8,243,045 – *Touch-sensitive display device and method*, August 14, 2012
U.S. Pat. 8,244,982 – *Allocating processor cores with cache memory associativity*, August 14, 2012
U.S. Pat. 8,260,996 – *Interrupt Optimization for Multiprocessors*, Sept. 4, 2012
101185761 (KR) – *Noise Cancellation for Phone Conversation*, Sept. 19, 2012
101200740 (KR) – *OLED display and sensor*, November 7, 2012
101200741 (KR) – T*ouch-sensitive display device and method*, November 7, 2012
U.S. Pat. 8,321,614 – *Dynamic scheduling interrupt controller for multiprocessors*, Nov. 27, 2012
U.S. Pat. 8,352,679 – *Selectively securing data and/or erasing secure data caches responsive to security compromising conditions*, Jan. 8, 2013
U.S. Pat. 8,355,541 – *Texture Sensing*, Jan. 15, 2013
U.S. Pat. 8,370,307 – *Cloud Data Backup Storage Manager*, Feb. 5, 2013
U.S. Pat. 8,398,451 – *Tactile Input Interaction*, March. 19, 2013
JP 5241032 B2 – *Routing Across Multicore Network Using Real World or Modeled Data*, April 13, 2013
ZL201010124820.3 – *Interrupt Optimization for Multiprocessors*, April 17, 2013
U.S. Pat. 8,428,438 – *Apparatus for Viewing Television with Pause Capability*, April 23, 2013
JP 5266197 B2 – *Data Centers Task Mapping*, May 10, 2013
U.S. Pat. 8,508,498 – *Direction and Force Sensing Input Device*, August 13, 2013
U.S. Pat. 8,547,457 – *Camera Flash Mitigation*, October 1, 2013
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101319048 (KR) – *Camera Flash Mitigation*, October 10, 2013
U.S. Pat. 8,628,478 – *Microphone for remote health sensing*, January 14, 2014
101362017 (KR) – *Thread Shift: Allocating Threads to Cores*, Feb. 5, 2014
101361928 (KR) – *Cache Prefill on Thread Migration*, Feb. 5, 2014
101361945 (KR) – *Mapping Of Computer Threads onto Heterogeneous Resources*, Feb. 5, 2014
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U.S. Pat. 8,687,533 – *Energy Reservation in Power Limited Networks*, April 1, 2014
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ZL201010124826.0 – *Dynamic scheduling interrupt controller for multiprocessors*, May 14, 2014
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U.S. Pat. 8,738,949 – *Power Management for Processor*, May 27, 2014

U.S. Pat. 8,751,854 – *Processor Core Clock Rate Selection*, June 10, 2014
JP 5559891 B2 – *Thermal Management in Multi-Core Processor*, June 13, 2014
101414033 (KR) – *Dynamic Computation Allocation*, June 25, 2014
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101426341 (KR) – *Processor core communication in multi-core processor*, May 23, 2014
U.S. Pat. 8,799,671 – *Techniques for Detecting Encrypted Data*, Aug 5, 2014
101433485 (KR) – *Task Scheduling Based on Financial Impact*, Aug. 18, 2014
U.S. Pat. 8,824,666 – *Noise Cancellation for Phone Conversation*, Sept. 2, 2014
U.S. Pat. 8,836,516 – *Snoring Treatment*, Sept. 16, 2014
U.S. Pat. 8,838,370 – *Traffic flow model to provide traffic flow information*, Sept. 16, 2014
U.S. Pat. 8,838,797 – *Dynamic Computation Allocation*, Sept. 16, 2014
U.S. Pat. 8,854,379 – *Routing Across Multicore Networks Using Real World or Modeled Data*, Oct. 7, 2014
JP 5615361 B2 – *Thread Shift: Allocating Threads to Cores*, Oct. 15, 2014
U.S. Pat. 8,866,621 – *Sudden infant death prevention clothing*, Oct. 21, 2014
U.S. Pat. 8,881,157 – *Allocating threads to cores based on threads falling behind threads*, Nov. 4, 2014
ZL201080024755.5 – *Camera Flash Mitigation*, Nov 5, 2014
U.S. Pat. 8,882,677 – *Microphone for remote health sensing*, Nov. 11, 2014
U.S. Pat. 8,924,743 – *Securing Data Cache through Encryption*, December 30, 2014
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HTC Corporation v. Telefonaktiebolaget LM Ericsson	E.D. Texas	6: 18-cv-00243-JRG
Seven Networks, LLC v ZTE (USA) Inc and ZTE Corporation	N. D. Texas - Dallas	3:17-CV-1495
AGIS Software Development, LLC v. HTC Corporation	E. D. Texas	2:17-cv-514
Barbaro Technologies, LLC v. Niantic, Inc	N.D. CA	3:18-cv-02955-RS
Immersion Corp. v. Samsung Electronics America, Inc. et al	E.D. Texas	2:17-cv-00572
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CISCO SYSTEMS, INC., vs. UNILOC USA, INC., UNILOC 2017 LLC and UNILOC LICENSING USA LLC	N.D. CA	3:18-cv-04991-SI
INTER PARTES REVIEW OF U.S. PATENT NO. 8,020,014 (Intel/VLSI)	PTAB	IPR2018-01661 IPR2018-01312
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Maxell, Ltd. et al v. VIZIO, Inc	C.D. CA	2-21-cv-06758
Inter Partes Review of U.S. Patent No. 7,619,912	PTAB	IPR2022-00615
Inter Partes Review of U.S. Patent Nos. 11,016,918 and 11,232,054	PTAB	IPR2022-00996 IPR2022-00999

APPENDIX B

AMERICAN NATIONAL STANDARD

ANSI/TIA/EIA-644-1995
Approved: November 15, 1995

TIA/EIA STANDARD

Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits

MARCH 1996

TIA/EIA-644

TELECOMMUNICATIONS INDUSTRY ASSOCIATION

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Representing the telecommunications industry
in association with the Electronic Industries Association

ELECTRONIC INDUSTRIES ASSOCIATION EIA EST. 1924

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(From Standards Proposal No. 3357, formulated under the cognizance of the TR-30.2 Subcommittee on DTE-DCE Interfaces.)

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Standards and Technology Department
2500 Wilson Boulevard
Arlington, VA 22201

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ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS

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FOREWORD

(This foreword is not part of this Standard)

This Standard was formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces.

This Standard specifies low voltage differential signaling (LVDS) generators and receivers capable of operating at data signaling rates up to 655 Mbit/s, devices may be designed for data signaling rates less than 655 Mbit/s, 100 Mbit/s for example, when economically required for that application.

This Standard was developed in response to a demand from the data communications community for a general purpose high speed interface standard for use in high throughput DTE-DCE interfaces.

The voltage levels specified in this Standard were specified such that maximum flexibility would be provided, while providing a low power, high speed, differential interface. Generator output characteristics are independent of power supply, and may be designed for standard +5 V, +3.3 V or even power supplies as low as +2.5 V. Integrated circuit technology may be BiCMOS, CMOS, or GaAs technology. The low voltage (330 mV) swing limits power dissipation, while also reducing radiation of EMI signals. Differential signaling provides multiple benefits over single-ended signaling, notably common mode rejection, and magnetic canceling.

The dc electrical levels are similar to electrical levels described in the IEEE 1596.3 standard, and will inter-operate at certain data signaling rates.

This Standard includes two annexes, both are informative only. Annex A provides guidelines for application, addressing data signaling rate and cable length issues. Annex B provides comparison information with other interface standards, and references to this Standard.

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1 SCOPE

This Standard specifies the electrical characteristics of low voltage differential signaling interface circuits, normally implemented in integrated circuit technology, that may be employed when specified for the interchange of binary signals between:

Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE),

Data Terminal Equipment (DTE) and Data Terminal Equipment (DTE),

or in any point-to-point interconnection of binary signals between equipment.

The interface circuit includes a generator connected by a balanced interconnecting media to a load consisting of a termination impedance and a receiver(s). The interface configuration is an uncomplicated point-to-point interface. The electrical characteristics of the circuit are specified in terms of required voltage, and current values obtained from direct measurements of the generator and receiver (load) components at the interface points.

The logic function of the generator and the receiver is not defined by this Standard, as it is application dependent. The generators and receivers may be inverting, non-inverting, or may include other digital blocks such as parallel-to-serial or serial-to-parallel converters to boost the data signaling rate on the interchange circuit as required by the application.

Minimum performance requirements for the balanced interconnecting media are furnished. Guidance is given in annex A, A.2 with respect to limitations on data signaling rate imposed by the parameters of the cable length, attenuation, and crosstalk for individual installations for a typical cable media interface.

It is intended that this Standard will be referenced by other standards that specify the complete interface (i.e., connector, pin assignments, function) for applications where the electrical characteristics of a low voltage differential signaling interface circuit is required. This Standard does not specify other characteristics of the DTE-DCE interface (such as signal quality, protocol, bus structure, and/or timing) essential for proper operation across the interface.

When this Standard is referenced by other standards or specifications, it should be noted that certain options are available. The preparer of those standards and specifications must determine and specify those optional features that are required for that application.

2 NORMATIVE REFERENCES

The following Standard contains provisions which, through reference in this text, constitute provisions of this Standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this Standard are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below. ANSI and TIA maintain registers of currently valid national standards published by them.

ANSI/TIA/EIA-422-B-1994 *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

EIA-485 *Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems*

ANSI/TIA/EIA-612-1993 *Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s*

3 DEFINITIONS, SYMBOLS AND ABBREVIATIONS

For the purposes of this Standard, the following definitions, symbols and abbreviations apply:

3.1 Data signaling rate

Data signaling rate, expressed in the units bit/s (bits per second), is the significant parameter. It may be different from the equipment's data transfer rate, which employs the same units. Data signaling rate is defined as 1/tui where tui is the minimum interval between two significant instants.

3.2 DTE

Data Terminal Equipment

3.3 DCE

Data Circuit-Terminating Equipment

3.4 LVDS

Low Voltage Differential Signaling

3.5 Star (*)

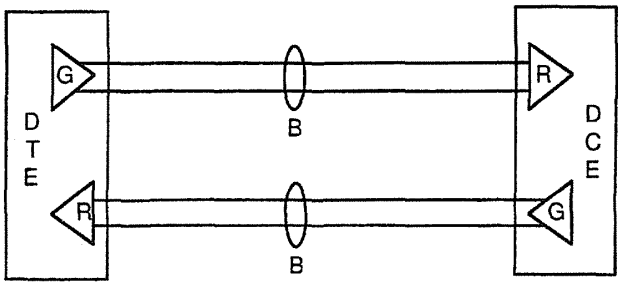
Star (*) - represents the opposite input condition for a parameter. For example, the symbol Q represents the receiver output state for one input condition, while Q* represents the output state for the opposite input state.

4 APPLICABILITY

4.1 General applicability

The provisions of this Standard may be applied to the circuits employed at the interface between equipments where information being conveyed is in the form of binary signals.

Typical points of applicability for this Standard are depicted in figure 1.



Legend:
DTE = Data Terminal Equipment
DCE = Data Circuit-termination Equipment
G = Generator
R = Receiver
B = Balanced interconnecting media

Figure 1 - Application of LVDS interface circuits

The LVDS interface is intended for use where any of the following conditions prevail:

a. The data signaling rate is too great for effective unbalanced (single-ended) operation.

b. The data signaling rate exceeds the capability of TIA/EIA-422-B, EIA-485, or TIA/EIA-612 balanced (differential) electrical interfaces.

c. The balanced interconnecting media is exposed to extraneous noise sources that may cause an unwanted voltage up to ±1 V measured differentially between the signal conductor and circuit common at the load end of the cable with a 50 Ω resistor substituted for the generator.

d. It is necessary to minimize electromagnetic emissions and interference with other signals.

e. Inversion of the signals may be required; e.g., plus MARK to minus MARK may be obtained by inverting the balanced interconnecting media.

4.2 Data signaling rate

The LVDS interface circuit will normally be utilized on data and timing, or control circuits where the data signaling rate is up to a recommended maximum limit of 655 Mbit/s. This limit is determined by the generator transition time characteristics, the media characteristics, and the distance between the generator and the load. Certain applications may impose a different (lower or higher) limit for the maximum data signaling rate. This may be accomplished by specifying a different minimum generator transition time specification, a different percentage of transition time vs. unit interval at the load, or by a different assumption of the maximum balanced interconnecting media signal distortion which is length dependent.

The theoretical maximum limit is calculated at 1.923 Gbit/s, and is derived from a calculation of signal transition time at the load assuming a loss-less balanced interconnecting media. The recommended signal transition time (tr or tf) at the load should not exceed 0.5 of the unit interval to preserve signal quality. This Standard specifies that the transition time of the generator into a test load be 260 ps or slower. Therefore, with the fastest generator transition time, and a loss-less balanced interconnecting media, and applying the 0.5 restriction, yields a minimum unit interval of 520 ps or 1.923 Gbit/s theoretical maximum data signaling rate.

NOTES

1 - 655 Mbit/s is the maximum data signaling rate for a serial channel, and employing a parallel bus structure (4, 8, 16, 32, etc. - bus width) can easily extend the obtainable equivalent bit rate into the Gbit/s range.

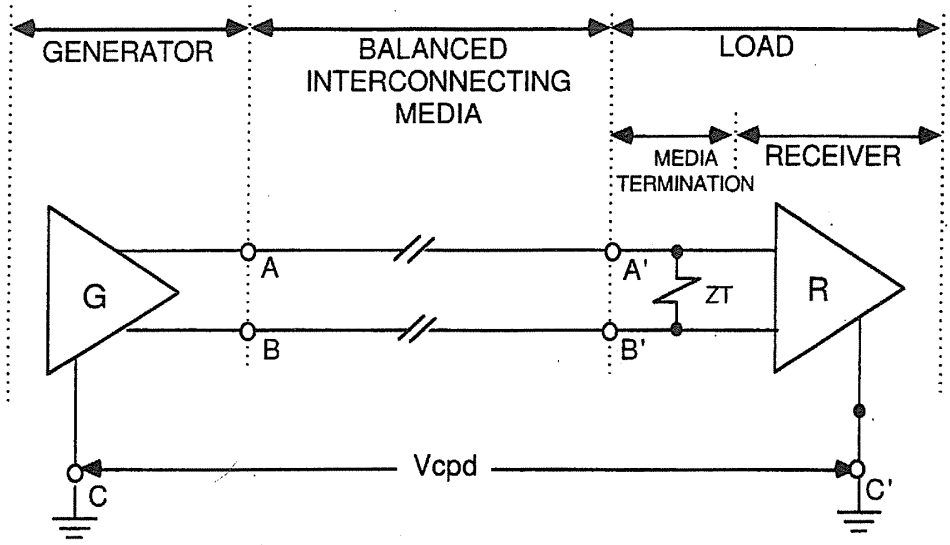
2 - The recommended maximum data signaling rate is derived from a calculation of signal transition time at the load. For example, if a cable media is selected, a maximum signal rise time degradation is assumed to be 500 ps, since cables are not loss-less (500 ps represents a typical amount of rise time distortion on 5 meters of cable media). Therefore, allowing a 500 ps degradation of the signal in the interconnecting cable yields a 760 ps (fastest) signal at the load. Therefore, with the fastest generator transition time, and a cable with only 500 ps of signal degradation (transition time), and applying the 0.5 restriction, yields a minimum unit interval of 1.520 ns or 655 Mbit/s recommended maximum data signaling rate.

Generators and receivers meeting this Standard need **not** operate over the entire data signaling rate range specified. They may be designed to operate over narrower ranges that satisfy more economically specified applications, for example at lower data signaling rates. When a generator is limited to a narrower range of data signaling rates, the transition time of the generator may be slowed accordingly to limit noise generation. For example, at 100 Mbit/s the generator's transition time should be in the range of 500 ps to 3 ns (5% to 30% of the unit interval), and the signal transition time at the load should not exceed 5 ns (50% of the unit interval).

While a restriction of maximum cable length in not specified, recommendations are given on how to determine the maximum data signaling rate for a typical cable media application (see A.2).

5 ELECTRICAL CHARACTERISTICS

The LVDS interface circuit is shown in figure 2. The circuit consists of three parts: the generator (G), the balanced interconnecting media, and the load. The load is composed of a termination impedance and a receiver(s) (R). The receiver may incorporate the termination impedance internal to the Integrated Circuit package. The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the balanced interconnecting media is described in terms of its electrical characteristics.



Legend:

G = Generator	R = Receiver
A = Generator interface point	A' = Receiver interface point
B = Generator interface point	B' = Receiver interface point
C = Generator circuit common	C' = Receiver circuit common

ZT = Termination impedance
Vcpd = Common potential difference

Figure 2 - LVDS interface circuit

5.1 Generator characteristics

The generator electrical characteristics are specified in accordance with the measurements illustrated in figures 4 to 8 and described in 5.1.1 through 5.1.4. The generator circuit meeting these requirements results in a balanced source that will produce a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV.

The signaling sense of the voltages appearing across the termination resistor is defined in figure 3 as follows:

a. The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 or OFF state.

b. The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 or ON state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

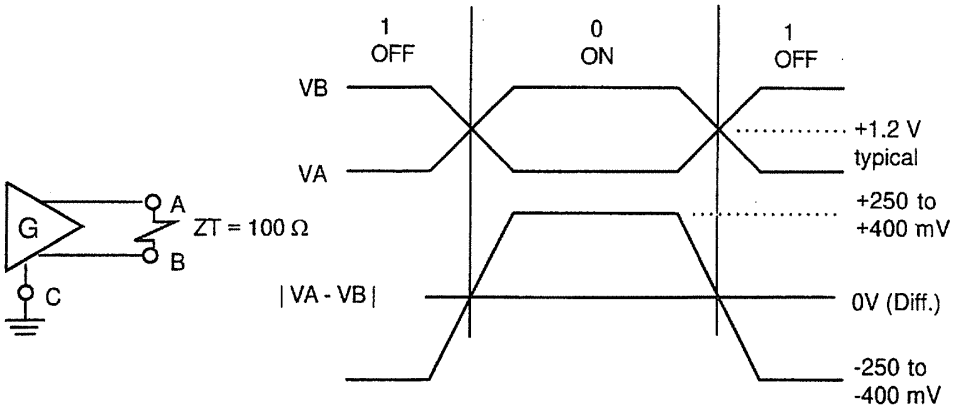


Figure 3 - Signaling sense

5.1.1 Test termination measurements (figure 4)

With a test load of two resistors, 49.9 Ω ±1% each, connected in series between the generator output terminals, the steady-state magnitude of the differential output voltage (Vt), shall be greater than or equal to 247 mV [99.8 Ω -1% (2.5 mA)] and less than or equal to 454 mV [99.8Ω +1% (4.5 mA)]. For the opposite binary state, the polarity of Vt shall be reversed (Vt*). The steady-state magnitude of the difference between Vt and Vt* shall be 50 mV or less.

$$\mathbf{247\ mV \le |\ Vt\ | \le 454\ mV}$$

$$\mathbf{247\ mV \le |\ Vt^*\ | \le 454\ mV}$$

$$\mathbf{|\ Vt\ | - |\ Vt^*\ | \le 50\ mV}$$

The steady-state magnitude of the generator offset voltage (Vos), measured between the center point of the test load and the generator circuit common shall be greater than or equal to 1.125 V and less than or equal to 1.375 V for either binary state. The steady-state magnitude of the difference of Vos for one binary state and Vos* for the opposite binary state shall be 50 mV or less.

$$\mathbf{1.125\ V \le Vos \le 1.375\ V}$$

$$\mathbf{1.125\ V \le Vos^* \le 1.375\ V}$$

$$\mathbf{|\ Vos\ | - |\ Vos^*\ | \le 50\ mV}$$

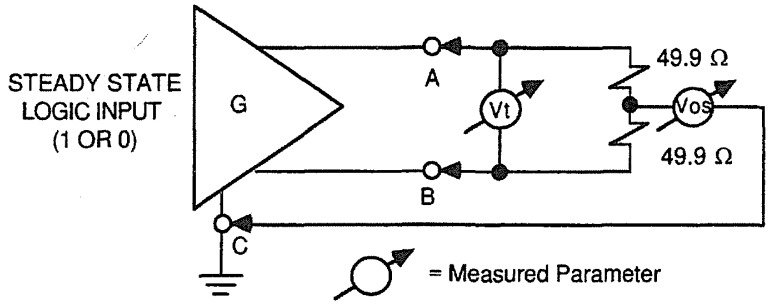


Figure 4 - Test termination measurements

5.1.2 Short-circuit measurements (figures 5, and 6)

With the generator output terminals short-circuited to the generator circuit common, the magnitudes of the currents (Isa and Isb) following through each output terminal shall not exceed 24.0 mA for either binary state (see figure 5).

$$|\ \mathbf{Isa}\ | \leq \mathbf{24.0\ mA}$$
$$|\ \mathbf{Isb}\ | \leq \mathbf{24.0\ mA}$$

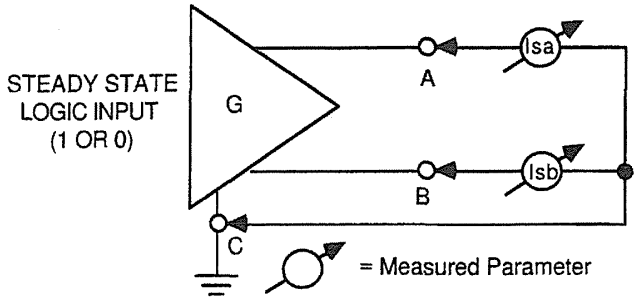


Figure 5 - Short-circuit measurements to circuit common

With the generator output terminals short-circuited to each other, the magnitude of the current (Isab) following through the output terminals shall not exceed 12.0 mA for either binary state (see figure 6).

$$|\ \mathbf{Isab}\ | \leq \mathbf{12.0\ mA}$$

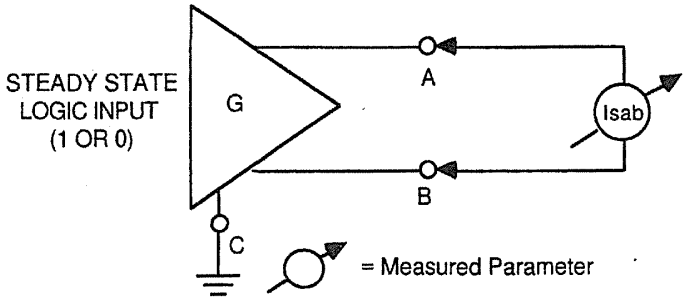


Figure 6 - Short-circuit measurements

5.1.3 Output signal waveform (figure 7)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across the 99.8 Ω ±1% test load (RL) and a maximum lumped capacitance test load of 5 pF (CL) connected as shown in figure 7, shall be such that the voltage monotonically changes between 0.2 and 0.8 of Vss and is less than or equal to 0.3 of the unit interval (at the maximum data signaling rate to be employed up to 200 Mbit/s). Above 200 Mbit/s the transition time shall be greater than or equal to 260 ps and less than or equal to 1.5 ns. Thereafter, the signal voltage shall not vary more than ±20% of the steady-state value (Vring), until the next binary transition occurs. Edge rates less than 260 ps are not recommended to minimize adverse effects of switching noise. Vss is defined as the voltage difference between the two steady-state values of the generator output (Vss = 2|Vt|). Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.

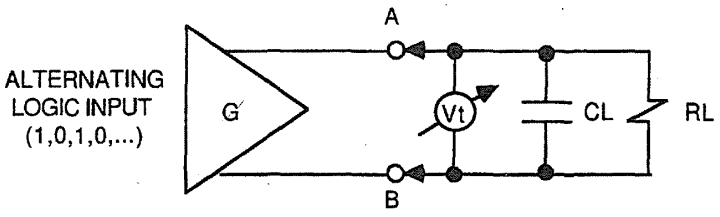
For data signaling rates ≤ 200 Mbit/s (tui ≥ 5 ns):

tr ≤ 0.3 tui, tf ≤ 0.3 tui

For data signaling rates ≥ 200 Mbit/s (tui ≤ 5 ns)

and ≤ 655 Mbit/s (tui ≥ 1.526 ns):

260 ps ≤ tr ≤ 1.5 ns, 260 ps ≤ tf ≤ 1.5 ns



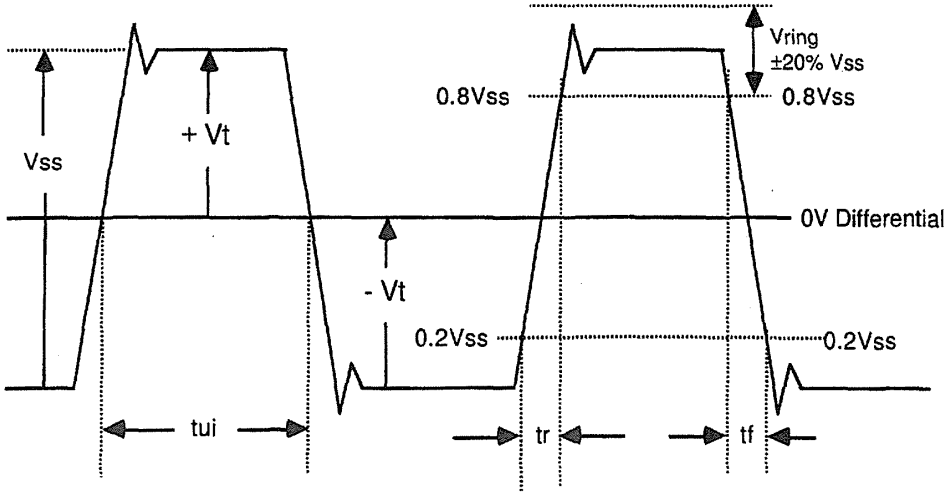


Figure 7 - Output signal waveform

5.1.4 Dynamic output signal balance (figure 8)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the resulting imbalance of the offset voltage (Vos) measured between the matched 49.9 Ω ±1% test load resistors (RL) to circuit common (C) and with a maximum lumped capacitance test load of 5 pF (CL) connected as shown in figure 8, should not vary more than 150 mVpp (peak-to-peak). Measurement equipment used for compliance testing shall provide a bandwidth of 1 GHz minimum.

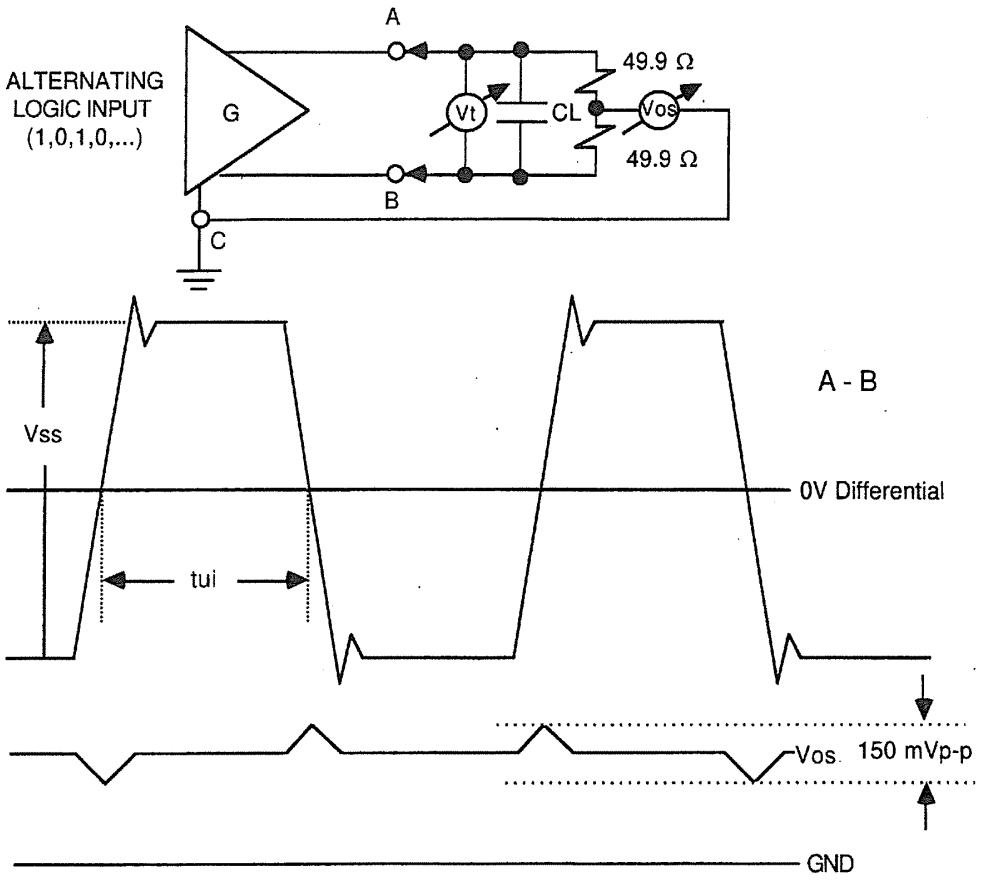


Figure 8 - Dynamic output signal balance waveform

5.2 Load characteristics

The load is defined as an impedance between A' and B' and is composed of a termination impedance and a receiver as shown in figure 2.

The electrical characteristics of a receiver without an internal termination impedance are specified in terms of measurements illustrated in figures 9, 12 and 13, and described in 5.2.1 and 5.2.3. Alternatively, the electrical characteristics of a receiver with an internal termination impedance is specified in terms of measurements illustrated in figures 10 to 13, and described in 5.2.2 through 5.2.3. A circuit meeting these requirements results in a differential receiver having a high input impedance (non-terminating receiver), and a small input threshold between ± 100 mV.

The media termination is specified in terms of measurements described in 5.2.4 and 5.2.2 for receivers that integrate the termination impedance.

The total load limit is specified in 5.4.3, and additional guidance is provided in 5.4.1 and 5.4.2 on multiple receiver operation and failsafe operation respectfully.

5.2.1 Receiver input current-voltage measurements (figure 9)

With the voltage Via (or Vib) ranging from 0 V to +2.4 V while Vib (or Via) is held at +1.2 V ± 50 mV, the resultant input current Iia (or Iib) shall be no greater than 20 μA in magnitude. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

> **NOTE 3 -** Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

$$|\ \mathbf{Iia}\ | \leq \mathbf{20}\ \mu\mathbf{A}$$
$$|\ \mathbf{Iib}\ | \leq \mathbf{20}\ \mu\mathbf{A}$$

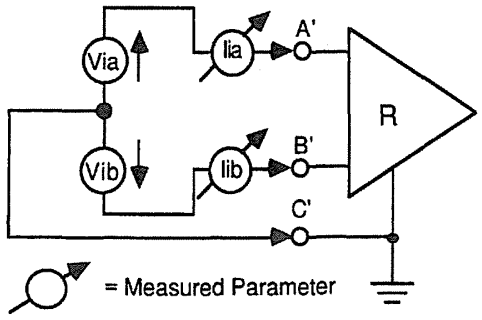


Figure 9 - Receiver input current-voltage measurements

5.2.2 Terminating receiver input current-voltage measurements and input impedance measurements (figures 10 and 11)

With the applied voltage (Vin) and forced current (Iin) listed in table 1 applied to the corresponding inputs, the resultant differential input voltage magnitude (Vid) shall be between the values listed in table 1. The test circuit is shown in figure 10 and applies only to receivers that provide an internal termination impedance. These measurements apply with the receiver's power supply in both power-on and power-off conditions.

NOTE 4 - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

$$\mathbf{225\ mV \leq |\ Vid\ | \leq 596\ mV}$$

Table 1 - Receiver input current-voltage measurements for terminating receivers

Applied Voltage Vin (V)	Forced Loop Current Iin (mA)	Switch Position S1 - S2	Resulting Input Voltage Vr (V)	Resulting Differential Input Voltage Range - Vid (mV)
2.4	- 2.5	A' - B'	2.070 to 2.175	+225 to +330
2.4	- 4.5	A' - B'	1.806 to 1.995	+405 to +596
2.4	- 2.5	B' - A'	2.070 to 2.175	-225 to -330
2.4	- 4.5	B' - A'	1.806 to 1.995	-405 to -596
0	- 2.5	A' - B'	0.225 to 0.330	-225 to -330
0	- 4.5	A' - B'	0.405 to 0.594	-405 to -596
0	- 2.5	B' - A'	0.225 to 0.330	+225 to +330
0	- 4.5	B' - A'	0.405 to 0.594	+405 to +596

NOTE 5 - Current into a terminal is positive, and current out of a terminal is negative.

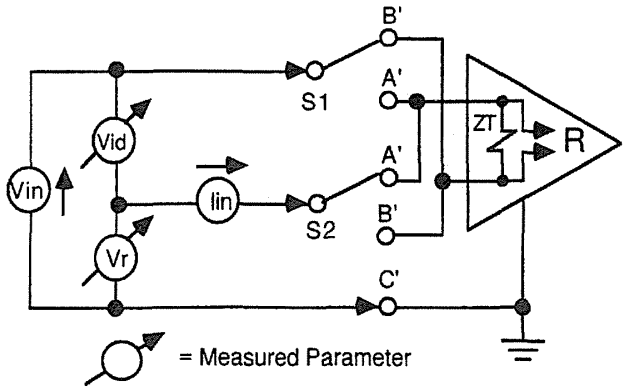


Figure 10 - Terminating receiver input current-voltage measurements

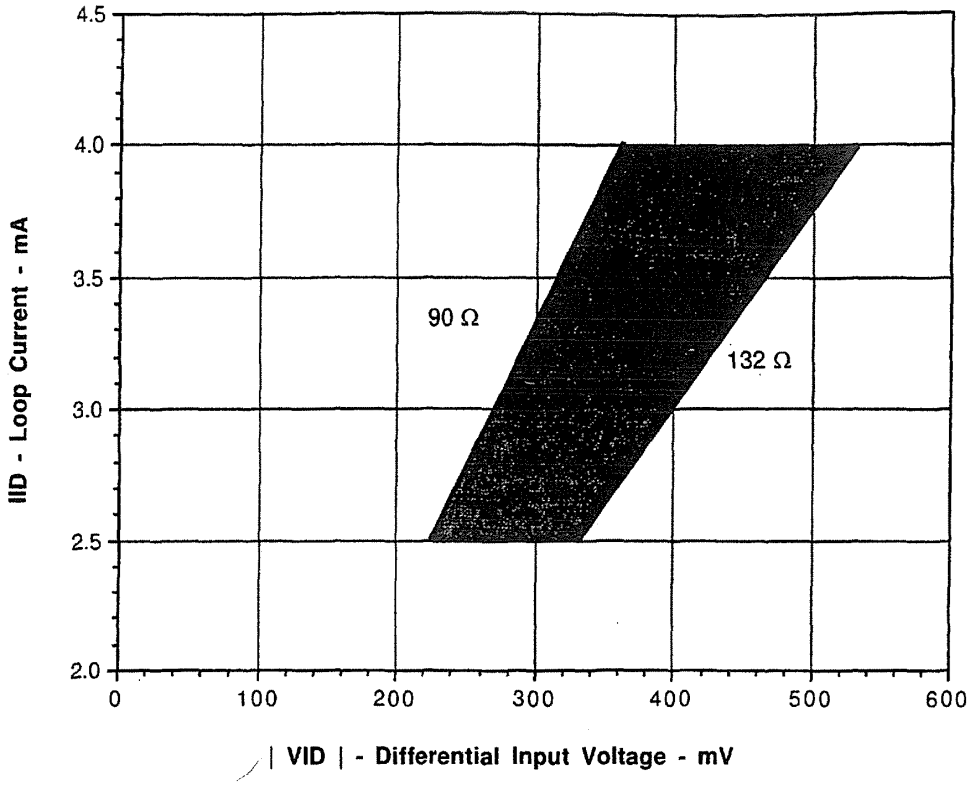


Figure 11 - Terminating receiver input current vs. input voltage range

The input impedance of the terminating receiver is dominated by the low impedance differential termination impedance (ZT). The resulting input impedance calculated from the measurements describe in table 1 shall be greater than or equal to 90 Ω, and less than or equal to 132 Ω. See 5.2.4 on media termination, and 5.4.3 on total load limit.

$$90\ \Omega \leq ZT \leq 132\ \Omega$$

NOTE 6 - The internal termination impedance may be a simple resistor incorporated into the package, integrated on the die, or composed of active devices on the die. The exact structure of the termination impedance is beyond the scope of this Standard.

5.2.3 Receiver input sensitivity measurements (figure 12)

Over an entire common mode voltage range of +0.050 V to +2.350 V (referenced to receiver circuit common), the receiver shall not require a differential input voltage of more than ±100 mV (threshold) to correctly assume the intended binary state. Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 100 mV and 600 mV in magnitude. The maximum voltage applied to either the A' or B' terminals shall not greater than +2.4 V, or be less than 0 V with respect to receiver circuit common. The maximum differential input voltage applied to the receiver is 2.4 V with no damage occurring to the receiver inputs.

Thresholds ≤ ±100 mV (differential)

100 mV ≤ Valid Differential Input Voltage Range ≤ 600 mV

0 V ≤ Valid Input Voltage (to circuit common) ≤ +2.4 V

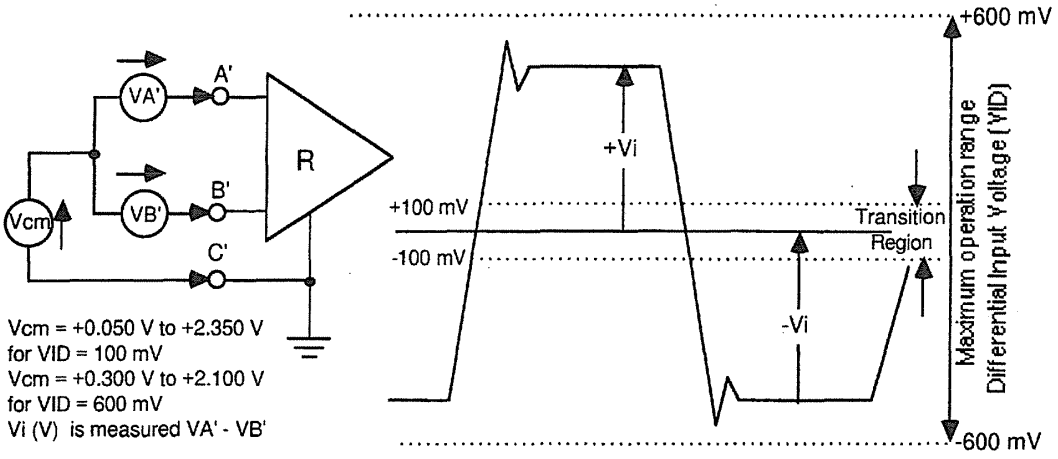


Figure 12 - Receiver input sensitivity measurements

Table 2 lists the minimum and maximum operating voltages of the receiver (input voltage, differential input voltage, and common mode input voltage), and the test circuit is shown in figure 13.

NOTE 7 - The logic function of the receiver is not defined by this Standard.

Table 2 - Receiver minimum and maximum operating voltages

Applied Voltages (Input Voltage - referenced to circuit common - C')		Resulting Differential Input Voltage VID	Resulting Common Mode Input Voltage VCM	Reason of Test
Via	Vib			
+1.250 V	+1.150 V	+100 mV	+1.200 V	To guarantee operation with minimum VID applied versus VCM range
+1.150 V	+1.250 V	-100 mV	+1.200 V	
+2.400 V	+2.300 V	+100 mV	+2.350 V	
+2.300 V	+2.400 V	-100 mV	+2.350 V	
+0.100 V	0 V	+100 mV	+0.050 V	
0 V	+0.100 V	-100 mV	+0.050 V	
+1.500 V	+0.900 V	+600 mV	+1.200 V	To guarantee operation with maximum VID applied versus VCM range
+0.900 V	+1.500 V	-600 mV	+1.200 V	
+2.400 V	+1.800 V	+600 mV	+2.100 V	
+1.800 V	+2.400 V	-600 mV	+2.100 V	
+0.600 V	0 V	+600 mV	+0.300 V	
0 V	+0.600 V	-600 mV	+0.300 V	

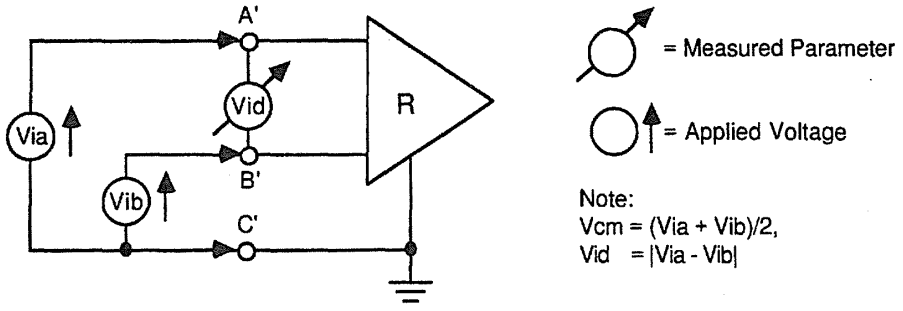


Figure 13 - Receiver input sensitivity test circuit

5.2.4 Media termination (figures 14 and 15)

All applications shall use a termination impedance. The recommended value is between 90 Ω and 132 Ω. The actual value should be selected to match the media characteristic impedance (±10%) at the application frequency. The termination impedance may be integrated onto the receiver integrated circuit, but subject to meeting the requirements of 5.2.2 instead of 5.2.1. If the termination impedance is not integrated into the receiver circuit, then it shall be located at the load end of the balanced interconnecting media, as close to the receiver input as possible to minimize the resulting stub length between the termination impedance and the receiver input.

NOTE 8 - Due to the high application frequency, care should be taken in choosing proper components such as the termination resistor, and in layout of the printed circuit board. The use of surface mount components is highly recommended to minimize parasitic inductance, and lead length of the termination resistor. Wire wound resistors are not recommended.

The value of this external impedance (ZT) is in the range of 90 Ω to 132 Ω. Ideally, the resistor value is equal to the characteristic impedance of the media or greater in value to minimize negative signal reflections. The media termination is shown in figures 14 and 15.

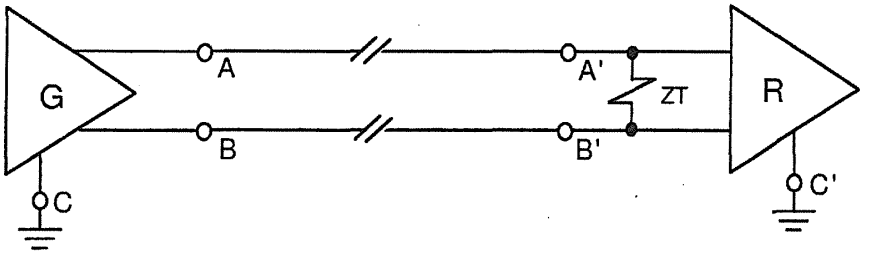


Figure 14 - Point-to-point application with external termination

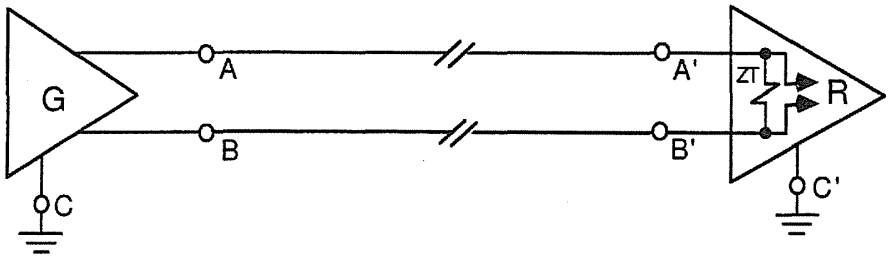


Figure 15 - Point-to-point application with internal termination

NOTE 9 - Matching of impedance of the PCB traces, connectors and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path should be minimized since they degrade the signal path and may cause reflections of the signal.

5.3 Interconnecting media electrical characteristics

The balanced interconnecting media shall consist of paired metallic conductors in any configuration which will maintain balanced signal transmission.

> **NOTE 10 -** The actual media of the cable is not specified and may be: twisted pair cable, twinax cable (parallel pair), flat ribbon cable, or PCB traces.

The performance of any balanced interconnecting media used shall be such to maintain the necessary signal quality for the specific application. If necessary for system consideration, shielding may be employed (see 8.2).

Annex A to this Standard provides guidance on performance and cable length versus data signaling rate and cable recommendations for typical cable applications.

5.3.1 Cable media

The cable media shall conform to the following electrical requirements:

5.3.1.1 Maximum dc loop resistance (DCR):

50 Ω is the maximum dc loop resistance of the cable. This corresponds to a voltage drop of 125 mV assuming minimum generator current of 2.5 mA.

5.3.1.2 Characteristic impedance:

110 Ω +/- 20% from 10 MHz to the application upper frequency limit.

5.3.1.3 Additional parameters

Additional parameters not specified which are application dependent (see Annex A) are: Maximum Attenuation, Maximum Propagation Delay, Maximum Propagation Delay Skew, Maximum Near End Crosstalk (NEXT), and Maximum Far End Crosstalk (FEXT). Crosstalk, skew, and related pair balance parameters may impact applications with multiple signal transmission lines.

5.3.2 PC Board trace media

The electrical requirements of PC Board traces shall also meet the requirements of 5.3.1.1 to 5.3.1.3.

5.3.3 Other media

It may be possible that other media may be employed, the definition and electrical characteristics of such media is beyond the scope of this Standard.

5.4 System parameters

5.4.1 Multiple receiver operation (figures 16 and 17)

The generator has the capability to furnish the dc signal necessary to drive multiple parallel connected receivers (without internal termination). However, the physical arrangement of the multiple receivers involves consideration of stub line lengths, location of the termination resistor, number of receivers, data signaling rate, circuit common, etc., that may degrade dynamic characteristics of the signal at the receivers if not properly implemented. It is recommended that stub lengths off the main line be as short as possible. In general, the propagation delay of the stub, should not exceed 15% of the signal transition time to prevent reflections and a severe impedance discontinuity. For applications with receivers without internal termination, the external termination resistor must be located at the far end (last receiver) of the interconnect. The actual arrangement must involve consideration of the aforementioned characteristics for the specific application and is therefore beyond the scope of this Standard. Figures 16 and 17 are provided for guidance only.

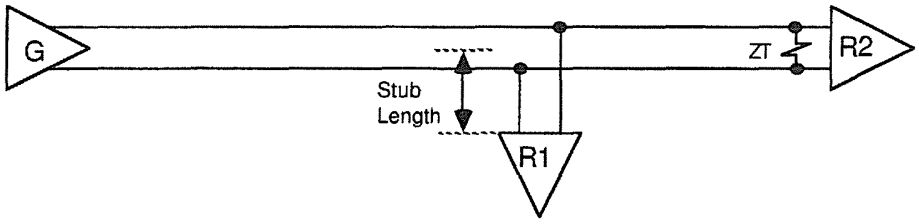


Figure 16 - Multiple receiver operation - multidrop application

NOTE 11 - If the configuration illustrated in figure 16 is employed, only the receiver at the far end of the cable may be a terminating receiver.

All receivers located between the generator and the final receiver must be non-terminating receiver(s). Multiple terminating receivers would present a low impedance load to the generator which would violate the total load limit (see 5.4.3), and adversely attenuate the signal.

The configuration shown in figure 17 is preferred over the multidrop configuration shown in figure 16. The configuration shown in figure 17 is composed of two independent uncomplicated point-to-point applications. At the expense of the second balanced interconnecting media, and termination impedance, the problem of stub lengths is eliminated, along with any impedance discontinuities that mid balanced interconnecting media connectors, and stubs may present. Signal quality is superior in an uncomplicated point-to-point configuration over a multidrop configuration.

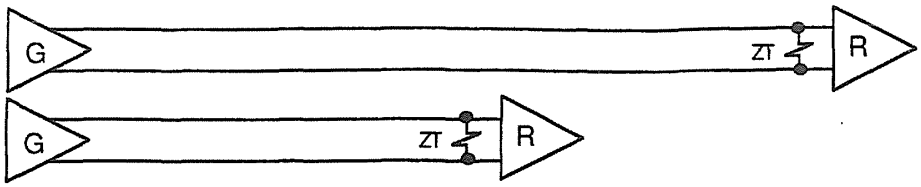


Figure 17 - Uncomplicated point-to-point application

5.4.2 Failsafe operation

Other standards and specifications using the electrical characteristics of the LVDS interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following:

1) generator in power-off condition
2) receiver not connected with the generator
3) open-circuited interconnecting cable
4) short-circuited interconnecting cable
5) input signal to the load remaining within the transition region (±100 mV) for an abnormal period of time (application dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified:

1) which interchange circuits require fault detection
2) what faults must be detected
3) what action must be taken when a fault is detected; the binary state that the receiver assumes
4) what is done does not violate this Standard

The method of detection of fault conditions is application dependent and is therefore not further specified as it is beyond the scope of this Standard.

5.4.3 Total load limit

The total load (ZL) including multiple receivers, failsafe provisions, and media termination shall have a total impedance greater than or equal to 90 Ω and less or equal to 132 Ω between its input points A' and B', shown in figure 2. The receiver(s) shall not require a differential input voltage of more than 100 mV in magnitude for all receiver(s) to assume the intended binary state.

$$\mathbf{90\ \Omega \leq ZL \leq 132\ \Omega}$$

6 ENVIRONMENTAL CONSTRAINTS

A LVDS interface circuit conforming to this Standard will perform satisfactorily at data signaling rates up to 655 Mbit/s providing that the following operational constraints are simultaneously satisfied:

a. For cable applications, the cable media meets the recommended cable characteristics, the cable length is within that recommended for the applicable data signaling rate indicated in annex A, A.2 and the cable is properly terminated.

b. For PC Board traces, the traces meets the recommended characteristics for the applicable data signaling rate, and the trace is properly terminated.

c. The input voltage at the receiver (with respect to receiver circuit common) is between 0 V and +2.4 V and either input (A' or B') terminal. The input voltage is defined to be any uncompensated combination of generator-receiver common potential difference, the generator offset voltage (Vos), and longitudinally coupled peak noise voltage.

d. Maximum common potential difference between the receiver circuit common and the generator circuit common is less than ±1 V.

7 CIRCUIT PROTECTION

The LVDS interface generator and receiver devices, under either the power-on or power-off condition, complying to this Standard shall not be damaged under the following conditions:

a. Generator open circuit.

b. Short-circuit across the balanced interconnecting media.

c. Short-circuit to common.

NOTE 12 - Some integrated circuit manufacturers may impose additional restrictions that may be required to meet this specification under the power-off condition.

8 OPTIONAL GROUNDING ARRANGEMENTS

8.1 Signal common (ground)

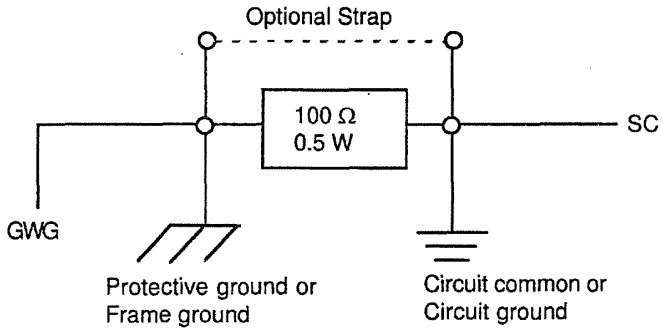
Proper operation of the LVDS interface circuits requires the presence of a signal common path between the circuit commons of the equipment at each end of the interconnection. The signal common interchange lead shall be connected to the circuit common which shall be connected to protective ground by any one of the following methods, shown in figures 18 and 19, as required by specific application.

The same configuration need not be used at both ends of an interconnection; however, care should be exercised to prevent establishment of ground loops carrying high currents.

8.1.1 Configuration "A" (figure 18)

The circuit common of the equipment is connected to protective ground, at one point only, by a 100 Ω ±20%, resistor with a power dissipation rating of 0.5 W. An additional provision may be made for the resistor to be bypassed with a strap to connect circuit common and protective ground directly together when specific installation conditions necessitate.

NOTE 13 - Under certain ground fault conditions in configuration "A", high ground currents may cause the resistor to fail; therefore, a provision shall be made for inspection and replacement of the resistor.

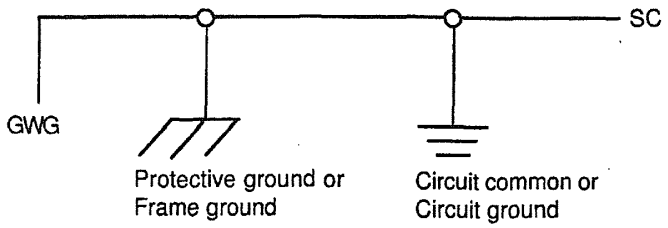


Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 18 - Optional grounding arrangements - configuration "A"

8.1.2 Configuration "B" (figure 19)

The circuit common shall be connected directly to protective ground.



Legend:
GWG = Green wire ground of power system
SC = Signal common interchange circuit

Figure 19 - Optional grounding arrangements - configuration "B"

8.2 Shield ground - cable applications

Some interface applications may require the use of shielded balanced interconnecting media for EMI or other purposes. When employed, the shield shall be connected only to frame ground at either or both ends depending on the specific application. The means of connection of the shield and any associated connector are beyond the scope of this Standard.

ANNEX A (informative)

GUIDELINES FOR CABLE APPLICATION

(This annex is not a formal part of the attached TIA/EIA Recommended Standard, but is included for information purposes only.)

A.1 Interconnecting cable

The following section provides further information to Section 5.3 and is additional guidance concerning operational constraints imposed by the cable media parameters of length and termination.

Generally, if more than one signal transmission line is required for an interface, twisted pairs are necessary to balance coupling reactance between individual conductors of adjacent pairs and thus reduce crosstalk.

A.1.1 Length

The length of the cable separating the generator and the load is based on a maximum loop resistance of 50 Ω, and a corresponding 125 mV loss of the signal.

The following examples given take only the dc effects into account in determining the maximum cable length. This would pertain to low speed operation only. The ac effects will limit the maximum cable length before the dc resistance for high speed applications. See A.2.

For the following cables gauges, the corresponding maximum length for a 50 mV signal loss is:

28 AWG	50 meters	(164 feet),
24 AWG	150 meters	(492 feet)

Longer lengths are possible, if the voltage attenuation is allowed to decrease the minimum generator differential output voltage to the maximum receiver threshold voltage (250 mV to 100 mV) for a 150 mV voltage attenuation or -7.9 dB. For the following cables gauges, the corresponding maximum length at a 150 mV signal loss is:

28 AWG	150 meters	(492 feet),
24 AWG	450 meters	(1,476 feet)

A.1.2 Typical cable characteristics

A.1.2.1 Parallel interface cable

The following characteristics apply to common parallel interface cable (as used for TIA/EIA-613, and other I/O interface standards) consisting of 25 twisted pairs surrounded by an overall shield:

A.1.2.1.1 Parallel cable, physical characteristics

Conductor	28 AWG, 7 strands of 36 AWG, tinned annealed copper, nominal diameter 0.38 mm (0.015 inch)
Insulation	Polyethylene or polypropylene; 0.24 mm (0.010 inch) nominal wall thickness; 0.86 mm (0.034 inch) outside diameter
Foil Shield	0.051 mm (0.002 inch) nominal thickness aluminum/polyester laminated tape helically wrapped around the core
Braid Shield	braided 36 AWG, tinned copper with 80% minimum coverage, in electrical contact with the aluminum surface of the foil shield
Diameter	nominal overall cable diameter 9.5 mm (0.375 inch)

A.1.2.1.2 Parallel cable, electrical characteristics

DC Resistance	221 Ω / km (67.5 Ω/1000 feet)
Mutual Capacitance	43 pF/m (13 pF/ft) at 1 kHz
Impedance	(characteristic, differential mode) 110 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.28 dB/m (0.085 dB/ft) at 50 MHz
Skew	(propagation delay) 0.115 ns/m (0.035 ns/ft)
Maximum Crosstalk	(Near End, NEXT) 30 dB at 50 MHz

A.1.2.2 Serial interface cable

The following characteristics apply to a common Category 5 serial interface cable (as used for TIA/EIA-422-B, and other I/O interface standards) consisting of 4 unshielded twisted pairs surrounded by an overall jacket:

A.1.2.2.1 Serial cable, physical characteristics

Conductor	24 AWG, 7 strands of 32 AWG, tinned annealed copper, nominal diameter 0.61 mm (0.024 inch)
Insulation	Polyethylene or polypropylene; 0.18 mm (0.007 inch) nominal wall thickness; 0.97 mm (0.038 inch) outside diameter
Foil Shield	optional
Braid Shield	optional
Diameter	nominal overall cable diameter 5.6 mm (0.22 inch)

A.1.2.2.2 Serial cable, electrical characteristics

DC Resistance	84.2 Ω / km (25.7 Ω/1000 feet)
Mutual Capacitance	48 pF/m (14.5 pF/ft) at 1 kHz
Impedance	(characteristic, differential mode) 100 Ω nominal at 50 MHz
Propagation Delay	4.8 ns/m (1.46 ns/ft)
Attenuation	0.17 dB/m (0.051 dB/ft) at 50 MHz
Maximum Crosstalk	(Near End, NEXT) 36.8 dB at 50 MHz

A.1.3 Cable termination

The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average 28 AWG, copper conductor, plastic insulated twisted pair cable, to a 50 MHz sine wave will be on the order of 110 Ω.

The range of 90 Ω to 132 Ω allows for a range of media characteristic impedance to be specified. The nominal media characteristic impedance is restricted to the range of 100 Ω to 120 Ω to allow for impedance variations within the media. Depending upon the balanced interconnecting media specified, the termination impedance should be within 10% of the nominal media characteristic impedance.

A.2 Cable length vs. data signaling rate guidelines

The maximum permissible length of cable separating the generator and the load is a function of data signaling rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and common potential differences introduced between the generator and the load circuit commons as well as by cable balance. Increasing the physical separation and the interconnecting cable length between the generator and the load interface points increases exposure to common mode noise, signal distortion, and the effects of cable imbalance. Accordingly, users are advised to restrict cable length to a minimum, consistent with the generator to load physical separation requirements.

To determine the maximum data signaling rate for a particular cable length the following calculations / testing is recommended. First, the maximum DCR of the cable length (loop resistance) should be calculated, then the resulting signal attenuation should be calculated at the load. The voltage at the load must be greater than the receiver thresholds of 100 mV. For a conservative design, a maximum attenuation of 50 mV is recommended. Next eye patterns are recommended to determine the amount of jitter at the load at the application data signaling rate and comparing that to system requirements. Typically maximum allowable jitters tolerances range from 5% to 20% depending upon actual system requirements. This testing should be done in the actual application if possible, or in a test system that models the actual application as close as possible. Parameters that should be taken in account include: balanced interconnect media characteristics, termination, protocol and coding scheme, and worst case data patterns (pseudo random for example). The generator / receiver manufacturers and also the media manufacturers should provide additional guidance in predicting data signaling rate versus cable length curves for a particular generator / receiver and a particular media as this relationship is very dependent upon the actual characteristics of the selected devices and media.

When generators are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, shall be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply).

A.3 Co-directional and contra-directional timing information

With co-directional (same direction as data) timing, there are minimal problems with proper clocking of the data bits since the difference between data and clock edges is mostly the result of generator and receiver skew and not the transmission line.

With contra-directional timing, the user is advised that generator and receiver skew are not the only items to be taken into account. The cable delay and skew must also be considered.

In both cases the clock should transition as close to the center of the data bit as possible.

ANNEX B (informative)

B.1 Compatibility with other interface standards

The LVDS interface circuit is not intended for direct inter-operation with other interface electrical characteristics such as TIA/EIA-422-B, EIA-485, TIA/EIA-612, ITU-T (Formerly CCITT) Recommendation V.11, emitter coupled logic (ECL) or PECL.

Under certain conditions, inter-operation with circuits of some of the above interfaces may be possible but may require modification in the interface or within the equipment, or may require limitations on certain parameters (such as common mode range); therefore, satisfactory operation is not assured, and additional provisions not specified herein may be required.

B.1.1 Generator output levels (figure B.1)

A generator complying to this Standard features a differential current source capable of delivering a loop current in the range of 2.5 mA to 4.5 mA. When loaded with a 100 Ω load, the resulting differential voltage across the resistor will be at least 250 mV and less than 450 mV (Vt). The center point is typically +1.2 V (Vos). These voltages are depicted in figure B.1.

Any balanced receiver device that guarantees and input range of at least 0V to +2.4V, and thresholds of 200 mV or less may directly inter-operate with the generator specified by this Standard and total noise is less than 50 mV.

The balanced receiver specified by this Standard may inter-operate with other balanced generators specified by other standards along as the balanced generator does not violate the maximum receiver input voltage range, and develops a differential voltage of at least 100 mV, and not greater than 600 mV. Inter-operation with generators that provide a greater differential voltage may also be possible with the use of an attenuating circuit. The actual arrangement of such circuits is beyond the scope of this annex.

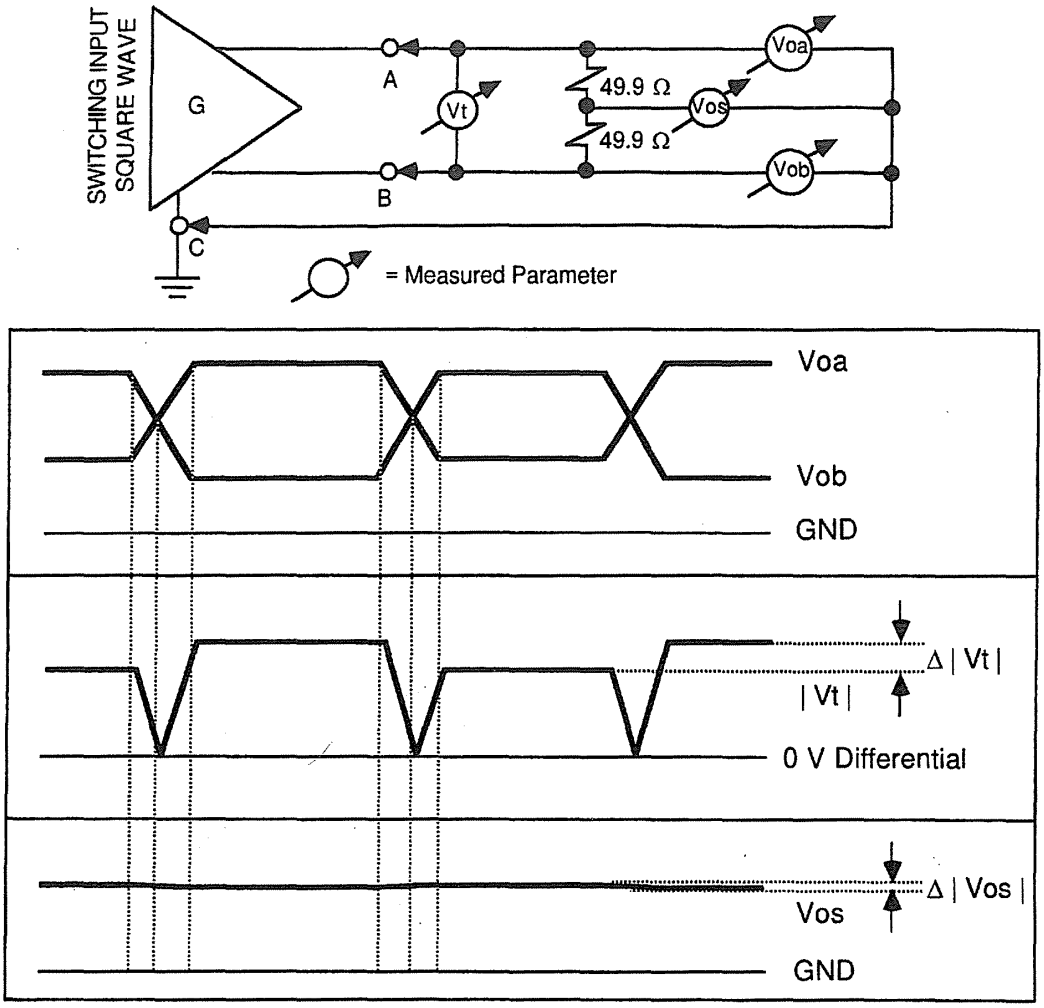


Figure B.1 - Generator output levels

B.1.2 Compatibility with IEEE 1596.3

This Standard features very similar DC electrical specifications to the IEEE 1596.3 standard titled: SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding. Direct inter-operation should be possible at certain data signaling rates without the use of intermediate circuitry. This Standard specifies generic electrical characteristics of low voltage differential signaling interface circuits for general purpose applications.

B.1.3 Compatibility with other interface standards

To determine whether direct inter-operation is possible with other interface standards, generator output levels and the receiver input specifications must be compared. Specifically the generator's differential output voltage, and offset voltage must be within the bounds of the receiver's input ranges. Correspondingly, the receiver's input thresholds and the input voltage range must be able to accept the generator's output levels. If this is the case, direct inter-operation is possible. If differences exists, additional provisions and or precautions may be required. This may include modification or additional circuitry inserted at the interface points or imposing limitations on certain parameters such as maximum common potential difference. The exact circuitry required is beyond the scope of this annex.

B.2 Power dissipation of generators

Power dissipation is greatly reduced within the generator circuits compared to other differential standards which specify a voltage mode generator. The current mode generator can produce less spike current during transitions compared to a voltage mode generator. As data signaling rate increases, this component becomes more critical. This allows for the generator to operate into the 300 MHz region without the use of special integrated circuit packages or heat sinks. The load signal is specified between 250 mV and 450 mV typically with a 100 Ω load, with creates a small loop current of only 2.5 to 4.5 mA compared to the minimum 20 mA loop current for a differential TIA/EIA-422-B generator. Since the load current component in also reduced, this allows for highly integrated generator / receiver devices to be offered in one package or integrated with other VLSI controller integrated circuits.

B.3 Related TIA/EIA standards

TIA/EIA-422-B *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*

EIA-485 *Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems*

TIA/EIA-612 *Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s*

B.4 Other related interface standards

IEEE 1596.3 *SCI-LVDS Low Voltage Differential Signals Specifications and Packet Encoding*

ITU-T (formerly CCITT) Recommendation V.11 *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications*

APPENDIX C

IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

Sponsor
Microprocessor and Microcomputer Standards Committee of the IEEE Computer Society

Approved 21 March 1996

IEEE Standards Board

Abstract: Scalable Coherent Interface (SCI), specified in IEEE Std 1596-1992, provides computer-bus-like services but uses a collection of fast point-to-point links instead of a physical bus in order to reach far higher speeds. The base specification defines differential ECL signals, which provide a high transfer rate (16 bits are transferred every 2 ns), but are inconvenient for some applications. IEEE Std 1596.3-1996, an extension to IEEE Std 1596-1992, defines a lower-voltage differential signal (as low as 250 mV swing) that is compatible with low-voltage CMOS, BiCMOS, and GaAs circuitry. The power dissipation of the transceivers is low, since only 2.5 mA is needed to generate this differential voltage across a 100 Ω termination resistance. Signal encoding is defined that allows transfer of SCI packets over data paths that are 4-, 8-, 32-, 64-, and 128-bits wide. Narrow data paths (4 to 8 bits) transferring data every 2 ns can provide sufficient bandwidth for many applications while reducing the physical size and cost of the interface. The wider paths may be needed for very-high-performance systems.
Keywords: backplane, bus, cable, differential, low-power, point-to-point, scalable, signal

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Introduction

[This introduction is not a part of IEEE Std 1596.3-1996, IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI).]

The demand for more processing power continues to increase, and apparently has no limit. One can usefully saturate the resources of any computer by merely specifying a finer mesh or higher resolution for the solution to a physical problem such as hydrodynamics or 3-D graphics. This demand leads engineers and scientists in a desperate search for more powerful and faster computers.

To economically obtain this kind of computing power, it seems necessary to use a large number of processors cooperatively. This cooperation is provided by the Scalable Coherent Interface (SCI), a high-speed packet transmission protocol that efficiently provides the functionality of bus-like transactions (read, write, lock, etc.). However, the initial physical implementations are based on emitter coupled logic (ECL) signal levels, which consume more power than is practical in the low-cost workstation environment. The initial specification's 1 Gbyte/s bandwidth (16-bit data path) may be overly expensive in the workstation environment. It may be more cost effective to use a narrower data path of sufficient bandwidth. The combination of a high-speed transmission environment and efficient protocols can provide the link for multiple processors to cooperate in a low-cost workstation environment.

The initial developers of this standard came from the Working Group that developed the SCI protocol (IEEE Std 1596-1992). The ECL signal levels defined for the SCI were effective in getting the standard implemented quickly and are practical for high-performance applications. They are less well suited, however, to using SCI in low-cost workstations. The obvious low-cost solution is to integrate the transceivers into the controller and implement both in CMOS. This integration will satisfy the space and power requirements of the workstation and personal computing market.

Eventually, a lower voltage swing will be needed in order to get higher speeds than ECL signal levels can provide. This standard can provide the basis for increasing parallel signal switching frequency into the gigahertz range.

Committee Membership

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CLAUSE PAGE

IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)

1. Overview

1.1 Scope

This standard specifies a process-technology-independent low-voltage (less than 1 V swing) point-to-point signal interface as optimized for IEEE Std 1596-1992 [B1],[1] which uses a differential driver connected to a terminated receiver through a constant-impedance transmission line. The interface will be optimized for CMOS processes, while being compatible with other IC processes, including GaAs and BiCMOS. The specification should support a transfer rate of at least 200 mega-transfers/second.

In addition, the specification will define encodings for transporting SCI packets over narrow and wide data paths (4-, 8-, 32-, 64-, and 128-bits, rather than the 16 bits defined by IEEE Std 1596-1992) using these signals.

1.2 Objectives

The primary goal of this standard is to create a physical layer specification for drivers and receivers and signal encoding suitable for use with the SCI as specified by IEEE Std 1596-1992 in low-cost workstation and personal computer applications. Other objectives include the following:

- *Technology independence*. Specifications should allow designs to be implemented in a variety of integrated-circuit technologies.
- *CMOS compatible*. Signal voltage levels and other specifications should be compatible with digital CMOS processes operating from 2 V through 5 V power supply levels.
- *Backplane and cable applications*. Specifications should be optimized for connections between boards contained within one chassis and short (less than 5 m) chassis-to-chassis interconnects. Longer connections are not prohibited, provided they meet specified signal loss and ground shift criteria for proper receiver operation. Connector and cable specifications are beyond the scope of this standard.
- *Scalable*. The original 16-bit-wide SCI data path should be supplemented by 4- and 8-bit-wide data paths to support a variety of cost/performance ratios. Support for 32-, 64-, and 128-bit-wide data paths will also be addressed.

[1] The numbers in brackets preceded by the letter B correspond to those of the bibliography in annex A.

1.3 Strategies

The basic design strategies selected by this standard include the following:

- *Low-voltage swing*. To minimize power dissipation and enable operation at very high-speed, low-swing (400 mV maximum) signals are specified.
- *Differential signals*. Small signal swings require differential signaling for adequate noise margin in practical systems.
- *Self-terminated*. To minimize board real estate and costs, and to maximize clock rates, each receiver is assumed to provide its own termination resistors.
- *Uniform ground*. The standard assumes that the ground potential difference between driver and receiver is kept small by the system design. The mechanism for constraining the ground potential difference is beyond the scope of this standard.

The most controversial decision was to use differential signals, which at first appears to double the number of signal lines. The pin-count overhead is actually much less than this, since reliable single-ended schemes require many more ground signals (many high-speed chips and/or backplanes provide one ground for every two signal pins) and run significantly slower. Other design benefits associated with differential signals include the following:

- *Constant driver current*. The transmitter consumes a (near) constant current when driving the links; the current remains the same, but is routed in the opposite direction when the signal value changes. This simplifies the design of power-distribution wiring.
- *Constant link current*. The net signaling current in a differential link is (nearly) constant, which greatly simplifies system design. The links are unidirectional and transmitters always drive a differential signal per table 2–1 or table 2–2. Reversing or stopping links would cause the net common-mode signaling current to change, creating system noise.
- *Low power*. A low signal current can be used, since much of the induced noise and ground-bounce appears as a common-mode signal.
- *Simple board design*. Although differential signals must be carefully routed on adjacent matched tracks, they are usually less sensitive to imperfections in the transmission line environment.
- *Low EMI*. Differential signals minimize the area between the signal and the return path. In addition, the equal and opposite currents create canceling electromagnetic fields. This dramatically reduces the electromagnetic emissions.
- *Low susceptibility to externally generated noise*. Though these links generate little noise, other parts of the system may. Differential signals are relatively immune to this noise.

1.4 Design models

1.4.1 Source-synchronous data

The SCI-LVDS link model assumes unidirectional operation (the driver always at one end of the link, the receiver at the other), and that a clock signal is sent along with the data as though it is just another data bit.

Both edges of the clock are used to delimit data, so the maximum transition rate of the clock is the same as the maximum transition rate of the data signals. This clock flows through the link at the same velocity as the data, and is to be used as the time reference for sampling the data.

In most applications, the received sampled data will need to be synchronized to the receiver’s local clock. If the transmitter’s clock and the receiver's clock are independent, and thus perhaps at slightly different frequencies, occasional symbols will need to be inserted or removed from time to time in an elasticity buffer in order to maintain synchronization.

The transmission system shall ensure that the setup and hold requirements of the receiving latches are met, in order to avoid incorrect data sampling and triggering metastable states. The receiver can observe the timing of the received clock relative to its own clock in order to choose an appropriate sampling time.

By carefully adhering to these assumptions, the SCI signaling protocol becomes independent of distance or delay. The maximum distance is limited by signal skew, caused by slight differences in propagation velocity from one signal to another, and by attenuation and distortion of the signals.

Because these signals are unidirectional, it is relatively easy to reshape and time-align them in order to transmit them greater distances. However, this may introduce timing jitter, which can make it impossible for the receiver to anticipate clock transitions with sufficient accuracy for reliable operation.

1.4.2 Terminated transmission lines

In addition to extending the signal encoding to parallel widths not included in IEEE Std 1596-1992, this standard specifies driver and receiver parameters only. However, a system must interconnect these components to be useful. The interconnect termination is specified in the receiver portion of this standard. The interconnect is beyond the scope of this standard because of the many options possible. The interconnect could include bond wires, packages and pins, printed circuit board, cables, connectors, multi-chip modules, wafer scale integration, or any combination of the previous options in one driver-to-receiver signal path. This signal path is important to the correct operation of a system implementing LVDS signals and is therefore discussed in general terms in this standard.

At the high data rates this standard supports, it is important to consider the transmission line aspects of the signal path. The high-frequency components of the 300 ps transition times make the parasitic reactive signal path components important. Familiar concepts, such as the receiver input capacitance, are overshadowed by the parasitic inductance of signal path elements that shape the waveform. If the signal delay through a signal path section is greater than the allowed minimum transition time, 300 ps, that section must be analyzed as a transmission line with associated characteristic impedance and delay. Impedance discontinuities through connectors, pins, solder pads, and bond wires to the IC itself cause reflections that degrade the signal integrity.

The receiver and its package input impedance need to match the signal transmission line impedance. This serves to minimize noise-causing reflections that create data errors. Given typical CMOS process tolerances, this generally implies the use of active devices to adjust the terminating resistance until it matches an external reference. Integrating the terminating impedance onto the receiver chip complicates the design and manufacturing, but the trade-off is simplified board layout and better signal integrity.

2. Document notation

2.1 Conformance levels

Several key words are used to differentiate between different levels of requirements and options, as follows:

2.1.1 expected: A key word used to describe the behavior of the hardware or software in the design models *assumed* by this specification. Other hardware and software design models may also be implemented.

2.1.2 may: A key word that indicates flexibility of choice with *no implied preference*.

2.1.3 shall: A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements to ensure interoperability.

2.1.4 should: A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended.*

2.2 Technical glossary

Many bus and interconnect-related technical terms are used in this document. These terms are defined below:

2.2.1 backplane: A board that holds the connectors into which SCI modules can be plugged. In ring-based SCI systems, the backplane may contain wiring that connects the output link of one module to the input link of the next. Usually the backplane provides power connections, power status information, and physical position information to the module.

2.2.2 board: The physical component that is inserted into one of the backplane slots. Note that a board may contain multiple nodes.

2.2.3 byte: Eight bits of data. *Syn:* **octet.**

2.2.4 differential voltage signal: The voltage difference between the true and complementary signals from a driver with two single-ended outputs whose signals always complement each other. Differential signals are also referred to as "balanced signals."

2.2.5 driver: An electrical circuit whose purpose is to signal a binary state for transmitting information. Also referred to as a "generator" in international standards.

2.2.6 flag: A signal used to delimit packets in parallel-signal-transmission implementations.

2.2.7 ground potential difference voltage: The voltage that results from current flow through the finite resistance and inductance between the receiver and driver circuit ground voltages.

2.2.8 idle symbol: A symbol that is not inside a packet and is therefore not protected by a CRC. Idle symbols serve to keep links running and synchronized when no other data are being transmitted. The idle symbol also contains flow-control information.

2.2.9 jitter: Refers to the time-uncertainty of a transitioning edge recurring in a repetitive signal. This uncertainty is only with respect to other edges in that signal. Jitter is commonly measured using random bit patterns and accumulating an eye pattern to show the worst-case difference in transitions.

2.2.10 LVDS: An abbreviation for low-voltage differential signal.

2.2.11 offset voltage: The driver offset voltage is the average dc voltage generated by the differential driver; $V_{os} = (V_{oa} + V_{ob}) / 2$.

2.2.12 packet: A collection of symbols that contains addressing information and is protected by a CRC. A subaction consists of two packets: a send packet and an echo packet.

2.2.13 physical interface: The circuitry that interfaces a module's nodes to the input link, output link, and miscellaneous signals.

2.2.14 receiver common-mode voltage: The combination of three components: 1) the driver-receiver ground potential difference (V_{gpd}); 2) the longitudinally coupled peak noise voltage measured between the receiver circuit ground and the signal transmission media with the driver end shorted to ground (V_{noise}); 3) the driver offset voltage.

2.2.15 receiver differential noise margin high: The tolerable signal voltage variation from any source that still results in the receiver producing a logic high output state when the driver is stimulated by a logic high input. Differential noise margin high is calculated by subtracting the receiver's minimum differential high input voltage from the driver's minimum high differential output voltage; $V_{odh}(\text{min}) - V_{idh}(\text{min})$.

2.2.16 receiver differential noise margin low: Tolerable voltage variation to guarantee that the receiver produces a logic low output when the driver is stimulated by a logic low input; $V_{idl}(\text{max}) - V_{odl}(\text{max})$.

2.2.17 SCI: *See:***Scalable Coherent Interface**

2.2.18 Scalable Coherent Interface (SCI): An abbreviation for the Scalable Coherent Interface standard, IEEE Std 1596-1992 .

2.2.19 signal line: An electrical or optical information-carrying facility, such as a differential pair of wires or an optical fiber, with associated driver and receiver, carrying binary true/false logic values.

2.2.20 skew: The difference in time that is unintentionally introduced between changing signal levels (incident edges) that occur on parallel signal lines. This difference results in an uncertain position with respect to time among parallel signals.

2.2.21 symbol: Refers to data within an SCI packet. A 16-bit unit of data accompanied by flag information. The flag information may be explicitly present as a 17th bit, or implied by the context. Symbols are transmitted one after another to form SCI packets or idles. The particular physical layer used to transmit these symbols is not visible to the logical layer.

2.2.22 sync packet: A special packet that is used heavily during initialization and occasionally during normal operation for the purpose of checking and adjusting receiver circuit timing.

3. Electrical specifications

3.1 Description and configuration

A LVDS interface, (figure 3-1), has a low-voltage swing (400 mV single-ended maximum), is connected point-to-point, and achieves a very high data rate (500 Mbits per second per signal pair) and reduced power dissipation. Power is low because signal swings are small: a minimum of 2.5 mA are sent through a 100 Ω termination resistor. This sharply reduced power dissipation enables an important advance: integrating the line termination resistors, interface drivers and receivers, and the processing logic in the same integrated circuit.

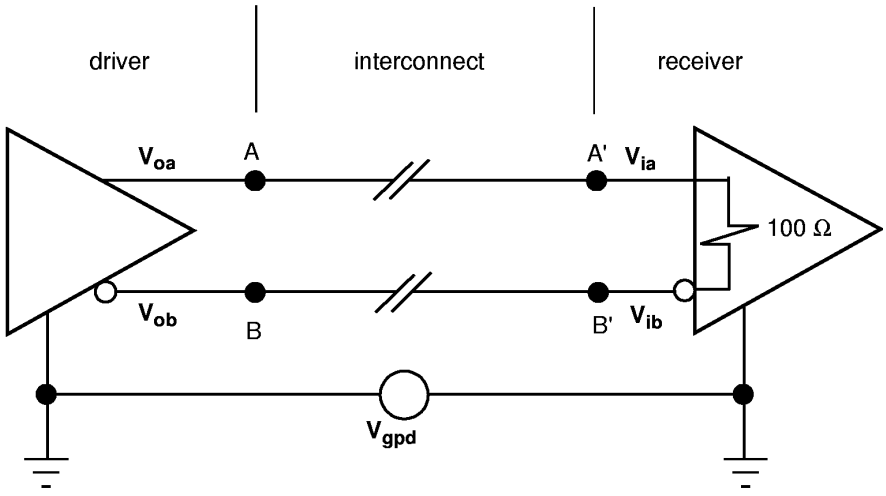


Figure 3-1 —LVDS interface

Switching speed is high because the driver load is an uncomplicated point-to-point 100 Ω transmission line environment. Switching speed is also high because interface devices are all on the same piece of semiconductor material, reducing the skew due to process, temperature, and supply variations between signal pairs. Connected in serial or parallel pairs, the LVDS interface forms a link used to transfer packets between integrated circuits, such as SCI nodes. For example, figure 3-2 shows circuit boards with LVDS links connected in a ring. The ring is implemented on a printed circuit board (PCB) similar in mechanical function to a multidrop bus backplane. The difference is that fewer PCB layers are needed to make the point- to-point connections. The PCB is simplified by eliminating the multidrop bus lines, as there is no need to route around interlayer vias used to make mechanical and electrical connections.

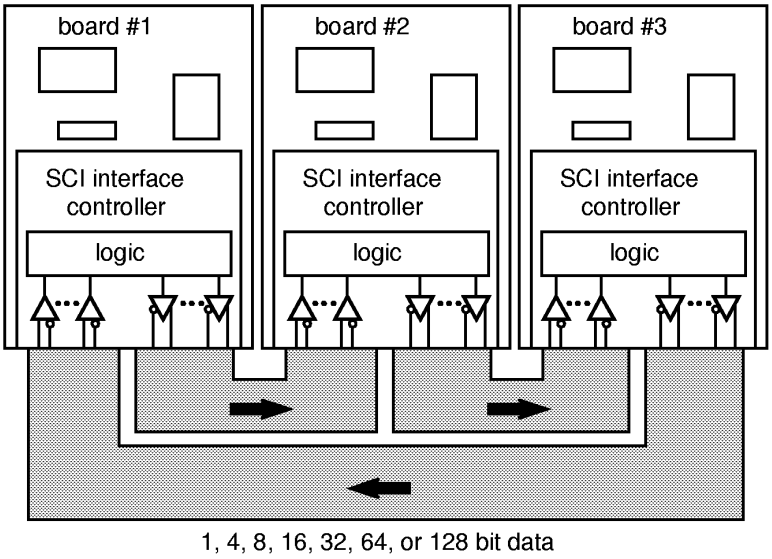


Figure 3-2 —Links in SCI application (ring connection)

LVDS is independent of the physical layer transmission media. As long as the media deliver the signals to the receiver with adequate noise margin and within the skew tolerance range, the interface will be reliable. This is a great advantage when using cables to carry LVDS signals. Since all connections are point-to-point, physical links between nodes are independent of other node connections in the same system. This allows for freedom in developing a useful interconnect that fits the needs of the application.

The data path can be serial or parallel with 1-, 4-, 8-, 16-, 32-, 64-, or 128-bits, depending on the needs of the user (see annex A, Signal encoding, for all widths except 1 and 16, which are defined in IEEE Std 1596-1992, clause 6, Physical layer).

Electrical specifications and skew specifications are optimized for 2–5 V supply voltages. The full range of semiconductor process technologies can be used to implement LVDS. It is intended that the specification be interoperable for all these technologies. The rapid trend toward reduced power supply voltage was considered in providing for signals that can be compatible with future system requirements.

The physical environment of point-to-point connections between circuit boards is further divided into two categories. The first (a general purpose link) is for circuit boards that need to operate with tolerance for V_{gpd} (table 3-1). This tolerance (approximately ± 1 V for a 2.5V powered system) is for a general purpose system. The second (a reduced-range link) is for boards mounted on a PCB or similar environment that will guarantee less than 50 mV V_{gpd} (table 3-2). In this environment, the differential signal is reduced by reducing the driver current. This reduces the power at both driver and receiver. This is a special consideration for subsystem implementations such as IEEE Std 1596.4-1994 RamLink.

The backplane environment implies short interconnects with controlled V_{gpd}. The use of cables implies that all the skew and signal quality requirements will be met by the cables, and the system designer will account for the worst-case V_{gpd} and provide appropriate safeguards. The scope of the electrical specification is the differential interface of drivers and receivers. The transmission media specification, whether cables or printed circuits, is beyond the scope of this standard.

3.2 Electrical specifications

The specification for driver and receiver parameters is given in table 3-1 and table 3-2. Descriptions of these parameters are contained in the following subclauses. These specifications shall be satisfied over the product's stated power supply voltage and temperature operating range.

Table 3-1 —General purpose link

Driver dc specifications:

Symbol	Parameter	Conditions	Min	Max	Units
V_{oh}	Output voltage high, V_{oa} or V_{ob}	R_{load} = 100 Ω ±1% Refer to figure 3-5		1475	mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	R_{load}= 100 Ω ±1%	925		mV
$\|V_{od}\|$	Output differential voltage	R_{load} = 100 Ω ±1%	250	400	mV
V_{os}	Output offset voltage	R_{load}=100 Ω ±1% Refer to figure 3-7	1125	1275	mV
R_o	Output impedance, single ended	V_{cm}=1.0 V and 1.4 V	40	140	Ω
ΔR_o	R_o mismatch between A & B	V_{cm}=1.0 V and 1.4 V		10	%
$\|\Delta V_{od}\|$	Change in $\|V_{od}\|$ between “0” and “1”	R_{load} = 100 Ω ±1%		25	mV
ΔV_{os}	Change in V_{os} between “0” and “1”	R_{load} = 100 Ω ±1%		25	mV
I_{sa}, I_{sb}	Output current	Driver shorted to ground		40	mA
I_{sab}	Output current	Drivers shorted together		12	mA
$\|I_{xa}\|$,$\|I_{xb}\|$	Power-off output leakage	V_{cc}=0 V		10	mA

Receiver dc specifications (all voltages are given with respect to receiver circuit ground voltage):

Symbol	Parameter	Conditions	Min	Max	Units
V_i	Input voltage range, V_{ia} or V_{ib}	$\|V_{gpd}\|$ < 925 mV	0	2400	mV
V_{idth}	Input differential threshold	$\|V_{gpd}\|$ < 925 mV	–100	+100	mV
V_{hyst}	Input differential hysteresis	V_{idthh}–V_{idthl}	25		mV
R_{in}	Receiver differential input impedance	—	90	110	Ω

Driver ac specifications:

Symbol	Parameter	Conditions	Min	Max	Units
Clock	Clock signal duty cycle	250 MHz	45	55	%
t_{fall}	V_{od} fall time, 20–80%	Z_{load} = 100 Ω ±1%	300	500	ps
t_{rise}	V_{od} rise time, 20–80%	Z_{load} = 100 Ω ±1%	300	500	ps
t_{skew1}	$\|tp_{HLA} - tp_{LHB}\|$ or $\|tp_{HLB} - tp_{LHA}\|$, Differential skew	Any differential pair on package*		50	ps
t_{skew2}	$\|tp_{diff}[m] - tp_{diff}[n]\|$ Channel-to-channel skew	Any two signals on package†		100	ps

Receiver ac specifications
(shall be maintained for 100 mV < *V*id < 400 mV throughout the receiver common-mode operating range):

Symbol	Parameter	Conditions	Min	Max	Units
t_{skew}	Skew tolerable at receiver input to meet set- up and hold time requirements	Any two package inputs		600	ps

*skew measurements are made at the 50% point of the transition.
†Skew measurements made at 0 V differential (the crossing of single-ended signals).

Table 3-2 —Reduced range link

Driver dc specifications (the ac specifications of table 3-1 apply without change for driver and receiver):

Symbol	Parameter	Conditions	Min	Max	Units
V_{oh}	Output voltage high, V_{oa} or V_{ob}	R_{load} = 100 Ω ±1% Refer to figure 3-5		1375	mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	R_{load} = 100 Ω ±1%	1025		mV
$\|V_{od}\|$	Output differential voltage	R_{load} = 100 Ω ±1%	150	250	mV
V_{os}	Output offset voltage	R_{load} = 100 Ω ±1% Refer to figure 3-7	1150	1250	mV
R_o	Output impedance, single ended	V_{cm}=1.0 V and 1.4 V	40	140	Ω
ΔR_o	R_o mismatch between A & B	V_{cm}=1.0 V and 1.4 V		10	%
$\|\Delta V_{od}\|$	Change in $\|V_{od}\|$ between “0” and “1”	R_{load} = 100 Ω ±1%		25	mV
ΔV_{os}	Change in V_{os} between “0” and “1”	R_{load} = 100 Ω ±1%		25	mV
I_{sa}, I_{sb}	Output current	Driver shorted to ground		40	mA
I_{sab}	Output current	Drivers shorted together		12	mA
$\|I_{xa}\|$,$\|I_{xb}\|$	Power-off output leakage	V_{cc}=0 V		10	mA

Receiver dc specifications (all voltages are given with respect to receiver circuit ground voltage):

Symbol	Parameter	Conditions	Min	Max	Units
V_i	Input voltage range, V_{ia} or V_{ib}	$\|V_{gpd}\|$ < 50 mV	825	1575	mV
V_{idth}	Input differential threshold	$\|V_{gpd}\|$ < 50 mV	–100	+100	mV
V_{hyst}	Input differential hysteresis	V_{idthh}–V_{idthl}	25		mV
R_{in}	Receiver differential input impedance	—	80	120	Ω

3.2.1 Driver output levels

The driver output, when properly terminated, results in a small-swing differential voltage. The relation between the single-ended outputs and the differential signal is shown in figure 3-3. The differential driver is made up from two single-ended outputs. These outputs alternate between sourcing and sinking a constant current. The differential voltage level is determined by the load resistance. The dc load seen by the driver is the receiver input impedance in parallel with the differential termination, 100 Ω, which dominates. The case where the current source is providing 4 mA is shown in figure 3-3, where the outputs are switching the current at a 50% duty cycle.

The receiver threshold limits are shown in figure 3-3, in relation to the single-ended signals that arrive at the receiver inputs. When the magnitude of the voltage difference exceeds the receiver threshold, then the receiver is in a determined logic state. For the purpose of this standard, a differential voltage greater than or equal to V_{idth}(max) is a logic high, and less than or equal to V_{idth}(min) is a logic low.

Ground shift margin is built in by confining the output to a range of V_{ol} to V_{oh} (e.g., this allows approximately 1 V of ground shift between a driver and receiver that are powered from 2.5 V supplies). Therange of allowable dc output levels for driver output voltages V_{oa} and V_{ob} is illustrated in figure 3-4. Measurement of the voltages V_{oa}, V_{ob} and the differential output voltage V_{od} is illustrated in figure 3-5.

The driver output shall always be terminated in compliance with this specification. The unterminated driver output voltage shall not exceed 2.4 V. Note that the receiver may be exposed to the unterminated driver output voltage briefly when a cable from the driver is being connected to the receiver—the cable will be charged to the unterminated driver output voltage.

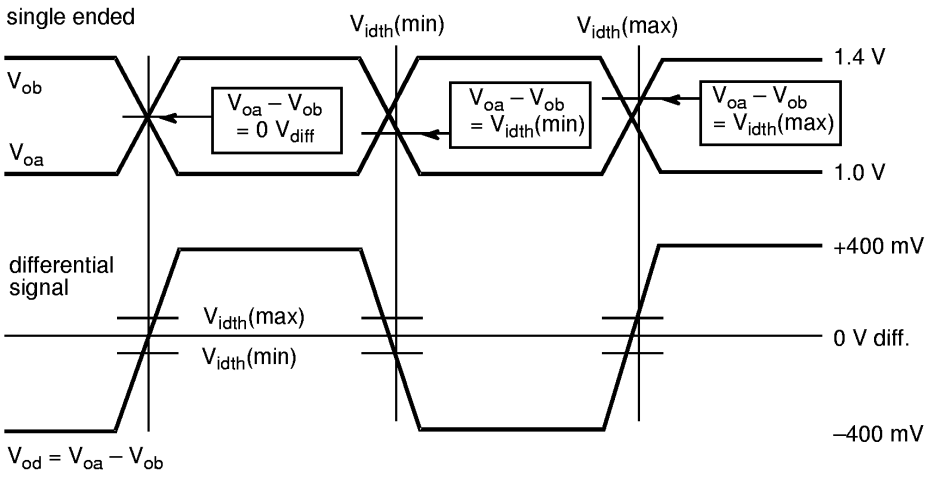


Figure 3-3 —Maximum driver signal levels shown for 1.2V V_{os}

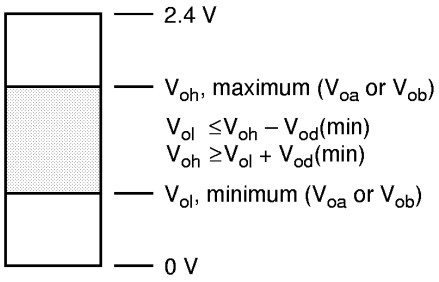


Figure 3-4 —Driver signal levels

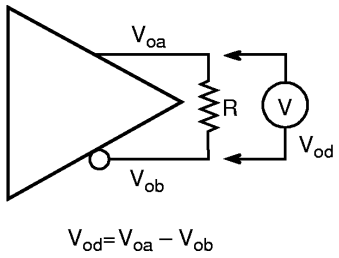


Figure 3-5 —Reference circuit

The following driver dc output voltage limits refer to figure 3-4 and figure 3-5, and shall apply for a load resistance R = 100 Ω connected as shown in figure 3-5.

Ideally, the amplitude and common-mode voltage of the steady-state differential output would not change, but in practical designs, both change. The output of a driver whose differential voltage (V_{od}) and driver offset voltage (V_{os}) change when the output changes state is shown in figure 3-6. The definition for V_{od} and V_{os} is shown in figure 3-7.

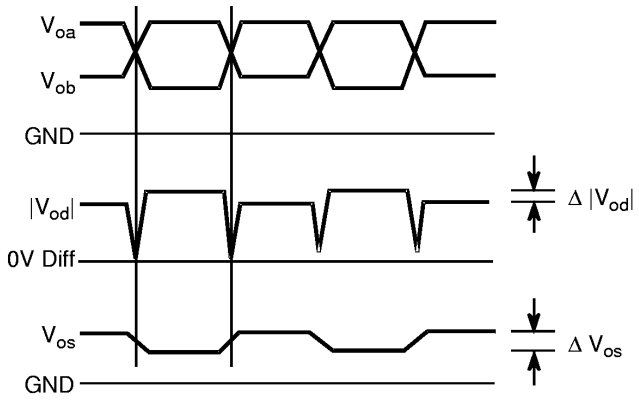


Figure 3-6 —Driver signal levels

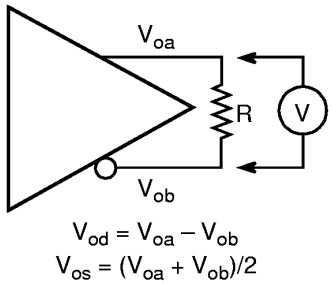


Figure 3-7 —Reference circuit

The definition of ΔV_{os} and ΔV_{od} are explicitly stated by taking into account the varying voltage levels of the single ended outputs when in the different logic states. This can be expressed by equation 1 and equation 2.

$$\Delta V_{OS} = \left|V_{OS}(\text{high}) + V_{OS}(\text{low})\right| \tag{1}$$

where

$V_{OS}(\text{high}) = (V_{oah} + V_{obl})/2$, and $V_{OS}(\text{low}) = (V_{oal} + V_{obh})/2$

$$\left|\Delta V_{od}\right| = \left|V_{od}(\text{high}) - \left|V_{od}\right|(\text{low})\right| \tag{2}$$

where

$V_{od}(\text{high}) = V_{oah} - V_{obl}$, and $V_{od}(\text{low}) = V_{obh} - V_{oal}$

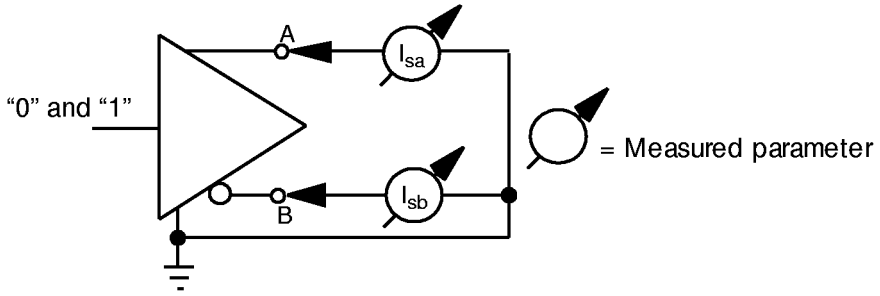
The driver dc output voltage limits refer to figure 3-6 and figure 3-7, and shall apply for a load resistance R = 100 Ω connected as shown in figure 3-7.

3.2.2 Driver short-circuit specification

To ensure that the driver circuit does not damage itself or other parts of the electronics, limits on the output currents when shorted mutually and to ground are imposed.

When the driver output terminals are short-circuited to the driver circuit ground, neither current magnitude(I_{sa} or I_{sb}) shall exceed the specified value in table 3-1 or table 3-2 as appropriate. The test circuit is shown in figure 3-8.

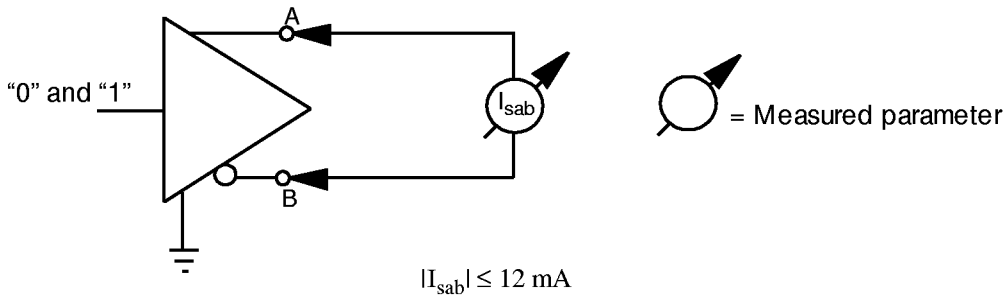
When the driver terminals are short-circuited to each other, the current magnitude shall not exceed the specified value in table 3-1 or table 3-2 as appropriate. The test circuit is shown in figure 3-9.



$|I_{sa}| \leq 24$ mA

$|I_{sb}| \leq 24$ mA

Figure 3-8 —Short-to-ground test circuit



$|I_{sab}| \leq 12$ mA

Figure 3-9 —Short-together test circuit

3.2.3 AC driver-output impedance

A difference between driver output impedance and signal path impedance causes reflections of incident edges arriving at the driver output from the transmission media. These waves that oppose the signal direction come from two sources: reflected signals and common-mode noise coupled onto the interconnect. To prevent common-mode noise reflected from the driver output from becoming a differential signal, the output impedance of the inverting and non-inverting outputs should be closely matched.

The upper limit of the output impedance should be as close to the transmission line impedance as possible. The lower limit on output impedance should not be much less than the impedance of the interconnect. An output impedance

significantly less than the interconnect impedance will generate negative differential reflections. The upper limit can be above the interconnect impedance; however, large reflections will cause ringing and noise problems on the lines. The amplitude of the reflected signal is the product of the incident wave amplitude and the reflection coefficient (ρ), as specified by equation 3.

$$V_{\text{reflected}} = \rho \times V_{\text{incident}} \tag{3}$$

The reflection coefficient is determined by the transmission line impedance and the driver output impedance, as specified in equation 4.

$$\rho = \frac{Z_d - Z_t}{Z_d + Z_t} = \frac{2(Z_d)}{Z_d + Z_t} - 1 \tag{4}$$

where

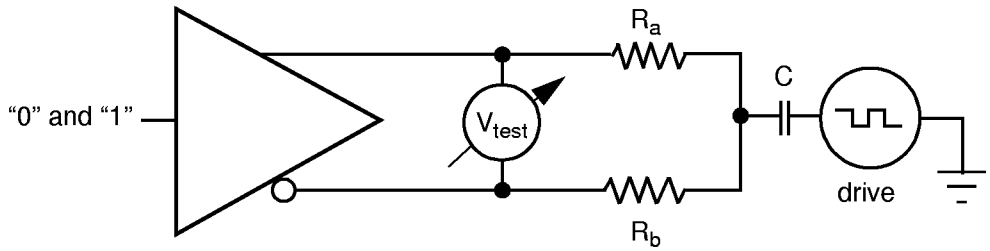
Z_t is transmission line impedance and Z_d is driver impedance. It follows that reflections less than 10% of the incident wave will result when equation 5 is satisfied.

$$0.1 > \left| \frac{2Z_t(Z_{outa} - Z_{outb})}{(Z_{outa} + Z_t)(Z_{outb} + Zt)} \right| \tag{5}$$

where

Z_{outa} and Z_{outb} are the respective output impedance of the complementary differential drivers.

Figure 3-10 illustrates a means of measuring the reflected voltage difference due to mismatched driver output impedance. The driver would be tested when driving differential high and then driving differential low. This is a means to test the dynamic output impedance, which may differ from the static output impedance. The dynamic impedance is important in the very high frequency operation for which the driver is designed to work. Since it is difficult to test the dynamic output impedance in a production environment, this parameter can be tested, verified, and guaranteed for a design.



$R_a = R_b = 50\ \Omega \pm 0.1\%$
$C = 0.033\ \mu F \pm 20\%$
drive = 500 mV peak to peak, 10 MHz
$|V_{test}| \leq 50$ mV peak to peak
(V_{test} is the differential voltage)

Figure 3-10 —Driver dynamic output impedance

3.2.4 DC driver-output impedance

Figure 3-11 illustrates a means of measuring the static driver output impedances, which have min/max as well as mismatch constraints. For each of the two possible output signal values (0 and 1), the output voltages shall be measured with driver-load common-mode (V_{cm}) voltages of 1.0 V and 1.4 V, yielding measured voltages of V_{oalo}, V_{oblo}, V_{oahi}, and V_{obhi}.

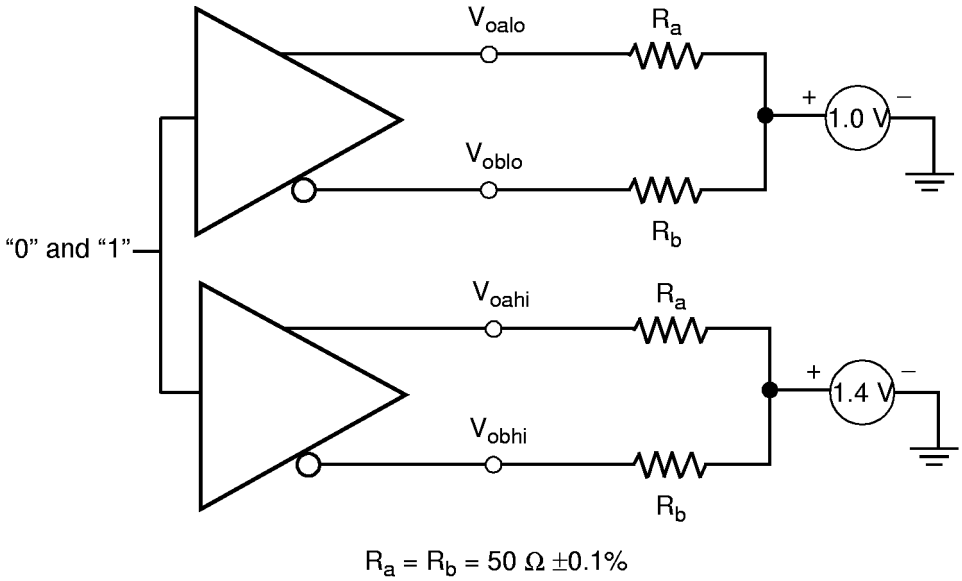


Figure 3-11 —Driver static output impedance

The values of these output voltages are based on the absolute and relative impedances of the drivers. The difference in a single output voltage (for 1.0 V and 1.4 V output-load voltages) is affected by the value of the driver's output impedance on this signal. The difference in the differential output voltages (for 1.0 V and 1.4 V output-load voltages) is affected by the matching of the driver's a and b output impedances. These values shall be within the constraints specified in table 3-3.

Table 3-3 —Static loaded-output voltage constraints

Parameter	Corresponds to	Units	Minimum	Maximum
V_{oahi}–V_{oalo}	R_o, terminal a	mV	178 (based on 40 Ω)	295 (based on 140 Ω)
V_{obhi}–V_{oblo}	R_o, terminal b			
$\lvert(V_{oahi}–V_{obhi})–(V_{oalo}–V_{oblo})\rvert$	10% matching of reflections coefficients	mV	0	20

3.2.5 Driver power-off leakage current

The driver output leakage currents (I_{xa} and I_{xb}) are measured under power-off conditions, V_{cc}=0 V, as shown in figure 3-12. With the voltage on the driver output terminals between 0 V and 2.4 V, with respect to driver common, these currents shall not exceed the value specified in table 3-1 or table 3-2.

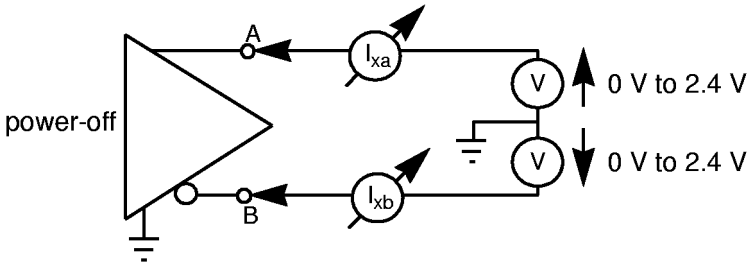


Figure 3-12 —Driver power-off leakage current test circuit

3.2.6 Receiver input levels

The receiver input signal is measured differentially, figure 3-13. The receiver output state is determined by a differential input signal greater than $+V_{idth}$ or less than $-V_{idth}$, within the permitted V_i range. The table 3-1 and table 3-2 receiver specifications are the same except for the common mode operating range and the on chip termination tolerance. The receiver common mode voltage input range, over which it must meet all other specifications, is reduced in table 3-2 because that is intended for operation in a well-controlled environment. The termination is allowed to have greater variance because it is intended to operate in a more controlled environment with less common-mode noise. For simplicity, the remaining receiver specification discussion here will apply directly to the general purpose specification. The analogous explanation will apply to the table 3-2 specification by substituting the appropriate numerical limits.

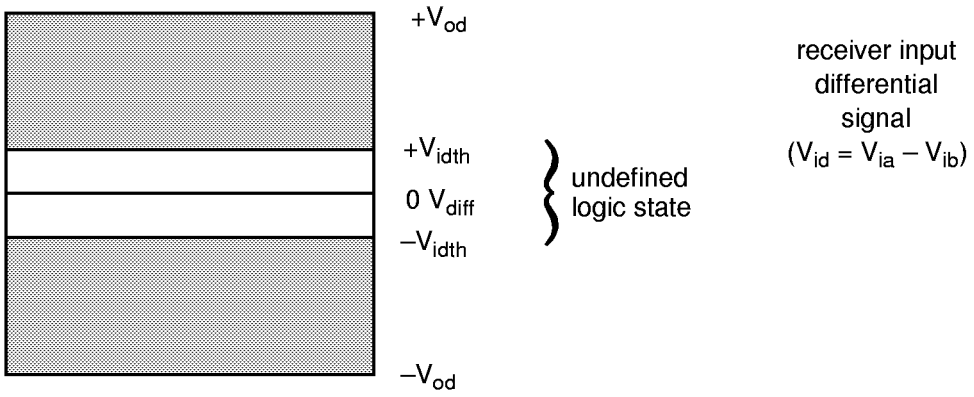


Figure 3-13 —Receiver signal levels, for table 3-1

The ability to accept voltages outside a V_i range is desirable because it increases noise immunity to ground potential difference and interconnect-coupled noise. The upper limit to the differential swing is given to ensure that receiver skew specifications are maintained for this range of input signals throughout the receiver common mode range. The range of allowable dc input levels for receiver input voltages, V_{ia} and V_{ib}, is illustrated in figure 3-14. Measurement of the voltages V_{ia}, V_{ib}, and the differential input voltage V_{id} is illustrated in figure 3-15.

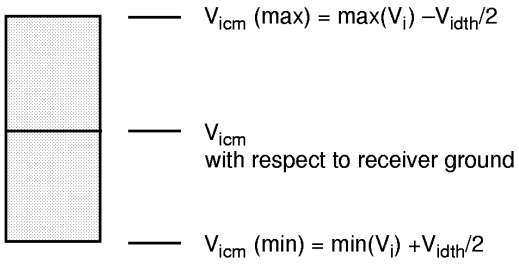


Figure 3-14 —Receiver signal common mode levels, table 3-1

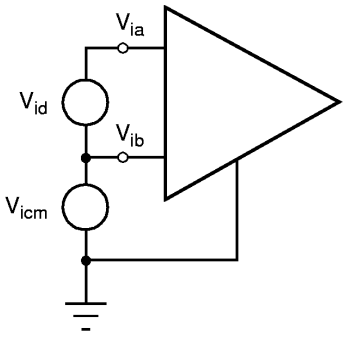


Figure 3-15 —Reference circuit

The signal common-mode level for table 3-1 is shown in figure 3-14. The receiver common-mode input voltage, V_{icm}, will be an alternating voltage depending on three superimposed conditions: the driver output condition, voltages induced on the interconnect, and reflections caused by common-mode termination imperfections.

This voltage can be expressed by accounting for the varying levels during both logic states. Equation 6 expresses the relationship of the four input voltages resulting from the three conditions previously stated.

$$V_{icm} = \frac{V_{ia} + V_{ib}}{2} \tag{6}$$

3.2.7 Receiver input impedance

A differential termination resistor (connected across the receiver inputs) should be integrated onto the receiver die. Integration is feasible because the power dissipated in the termination is less than 2 mW per receiver, and a single value can match the point-to-point interconnect characteristic impedance. Since an alternate termination scheme would be more useful in certain applications, there are modifications allowed to this requirement. For example, a common-mode termination to 1.2 V would be desirable when the ground potential difference between receiver and driver cannot be guaranteed to meet the limits specified in table 3-1. This allows the ground potential difference to be divided between the driver and the receiver. This common-mode termination can still use integrated termination resistance values of 50 Ω from each input to a common externally accessible pin. This does require an additional pin as shown in figure 3-16; however, all parallel channels can bus this common-mode termination together. Figure 3-16 shows both alternatives and defines the differential input impedance as the impedance measured across the receiver inputs.

Note that the receiver input capacitance should be designed to be as low as possible. Details of integrating the termination impedance are left to the circuit designer's discretion, but the termination should not limit the high-frequency, 250 MHz operation of the receiver.

The unpowered receiver impedance is not specified, since active circuits (which require power) are expected to be used to implement the on-chip termination resistance. However, when unpowered, the magnitude of the receiver’s leakage current (the sum of the two input currents) shall not exceed 1.0 mA.

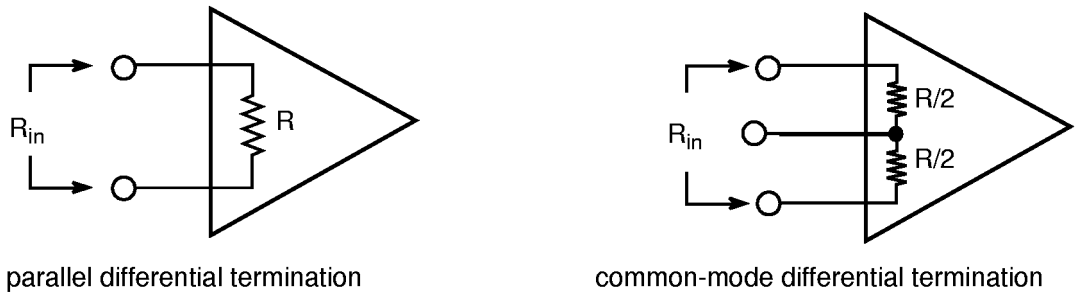


Figure 3-16 —Receiver input impedance

3.2.8 Receiver threshold hysteresis

The threshold hysteresis is important in receiver design to eliminate the possibility of oscillating receiver output when the differential input is undefined (see figure 3-17). The undefined input can occur when the receiver inputs are unconnected, when the connected driver is powered down, or when transitioning between defined values. The 25 mV minimum hysteresis means that an input signal must change by more than this value to change the receiver output state. A known output condition for an open or shorted receiver input (failsafe) is implementation-dependent and beyond the scope of this standard.

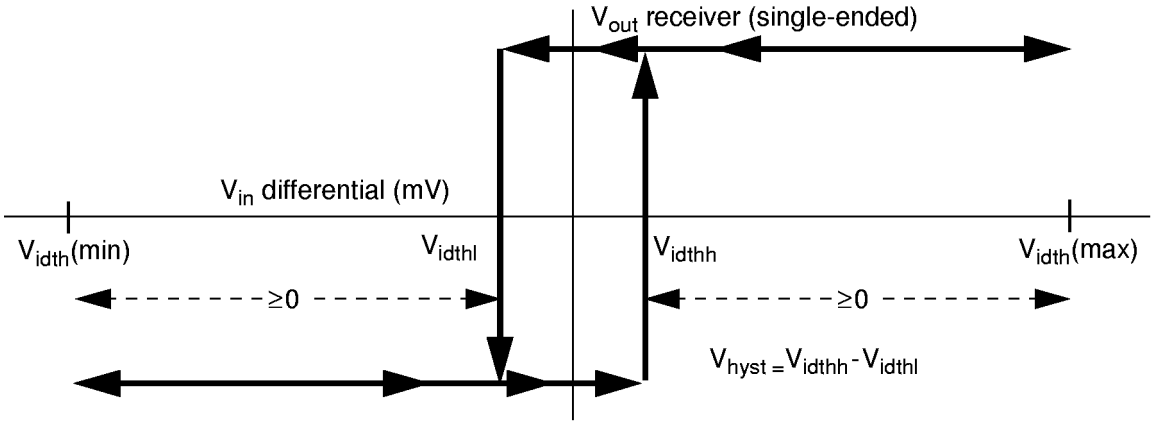


Figure 3-17 —Receiver hysteresis

3.3 AC specifications

A basic goal for this specification is to preserve the high transfer rate of the ECL physical layer (1 bit/2 ns for each differential signal pair) while drastically reducing power dissipation. The skew and transition time limits specified in this subclause correspond to those of the base SCI standard.

3.3.1 Driver transition times and undershoot

The 500 ps maximum transition time specified in this subclause is equivalent to a 0.3 V/ns slew rate for a 250 mV differential signal. This is the minimum guaranteed slew rate for the signals specified in this standard. The transition time is most critical through the receiver threshold region because the high-speed comparator design needs unambiguous inputs to function efficiently. The 0.3 V/ns slew rate in the threshold region shall guarantee reliable receiver switching.

The fast transitions contain high-frequency components that directly affect the electromagnetic radiation (EMR) created by the signal. Normally these high frequencies would create electromagnetic compatibility (EMC) problems. The differential signal advantage is produced by single-ended signals simultaneously rising and falling. These edges will generate equal and opposite electromagnetic fields that cancel each other and reduce generated fields and radiation. Therefore, it is important to have both single-ended channels switching at the same time and at the same slew rate; i.e., no skewed single-ended transitions.

Undershoot, overshoot, and fast rise times can generate noise, crosstalk, and electromagnetic interference. Although the driver specifications in figure 3-19 and figure 3-20 reduce these problems, careful transmission-line design is important to maintain signal integrity.

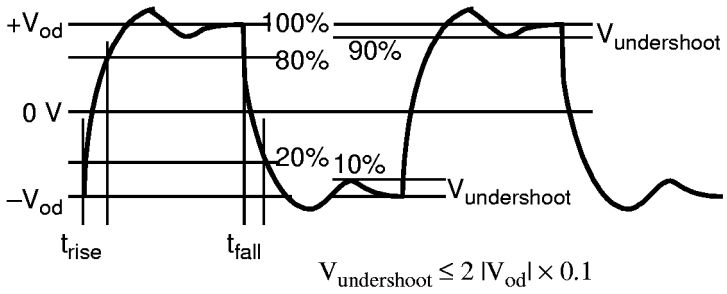


Figure 3-18 —Driver waveform

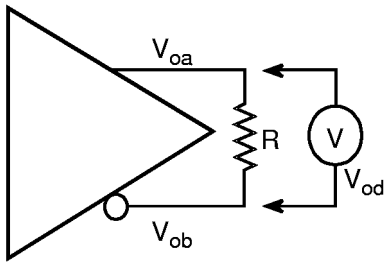


Figure 3-19 —Reference circuit

3.3.2 Receiver common-mode rejection

The receiver specified for table 3-1, the general purpose specification, is intended to operate over a common-mode voltage range that will allow for about ± 1 V ground-potential difference between the driver and receiver power supplies. The common-mode input voltage, V_{icm}, is the average of V_{ia} and V_{ib} measured with respect to the receiver ground potential. The equation expressing this value is given in 3.2.6. The receiver specified in table 3-1 and table 3-2 must maintain the sensitivity and skew specifications throughout this common-mode voltage range [see figure 3-14 for V_{icm}(max) and V_{icm}(min) definitions].

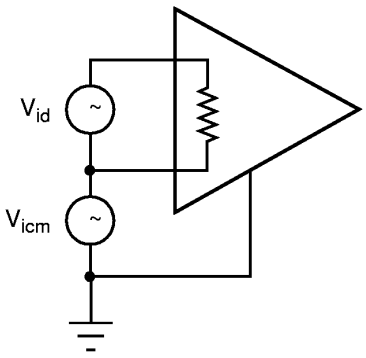


Figure 3-20 —V_{icm} reference circuit

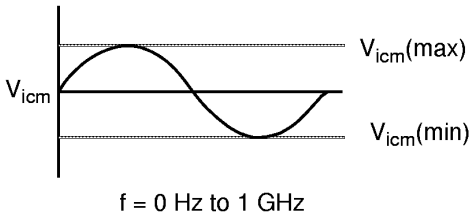


Figure 3-21 —V_{icm} input waveform

3.4 Skew specifications

System interconnects comprised of parallel signals must account for skew. This standard includes skew specifications because limiting skew is important for correct data transfers in a system. For example, the SCI physical system can be thought of as a data pipeline. Bytes of data can be lined up in the physical layer, a virtual FIFO. Since more than one transmission can be contained in the data path at any time, it is not the total delay time but the timing skew that is important to reliable SCI data transfer. The skew is extremely important because it directly affects the sample window (setup and hold time) available to the receiver logic. These skew specifications are based on a total allowable skew tolerance that will still provide an adequate sample window for receiver capture logic. Since the bit width is nominally 2 ns, reliable data transfer assumes that a 600 ps skew will be the maximum allowed.

The physical layer skew is defined for the purpose of this standard as the difference in time that is unintentionally introduced between changing signal levels (incident edges) that occur on parallel signal lines. This difference results in an uncertain position with respect to time between parallel signals. Jitter is not specified in this standard because the skew specification accounts for jitter as well. Jitter is the error of the time of transitions occurring in a serial transmission line. The range of parallel skew includes uncertainties that would be called jitter in a serial specification.

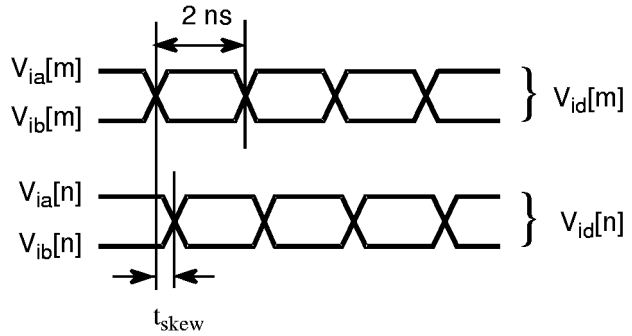
A parallel clock signal always accompanies SCI data signals. This clock is specified to be 250 MHz and to have a duty cycle that is greater than 45% and less than 55%. Since it would be impractical to force the circuit designer to vary the clock duty cycle to the minimum and maximum limits, testing would be done with the clock as generated. It would be tested under the same conditions as the data signals, since it is implied that they are on the same die. The requirement is for the clock to comply with the 45–55% duty cycle first, and then test all skew parameters to that clock. Since “any two signals” is specified for skew measurements, the relation of all signals to clock is implied because “any two” includes all pairs for skew measurement.

From the perspective of the receiver, the maximum clock-to-data signal skew is more important than the maximum data-to-data signal skew. However, from a manufacturing perspective, minimal skew design techniques are unlikely to treat the clock signal as special; therefore, skew measurements are not based upon it. Note that sophisticated receivers can measure min/max data-signal skews and dynamically adjust the clock signal delay, to reduce the effective clock-to-data skew to a little more than half of the “any-two” skew specification.

However, testing for the range of skew between the first and last signal may be inconvenient, so a more constraining specification could be used to simplify testing: require all data signals to be within ± 300 ps of the clock.

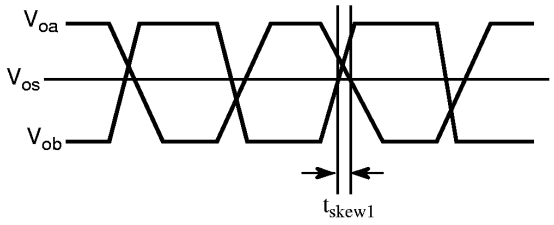
The physical transmission mechanisms do not differentiate between the clock and other signals, so any given transmission link might happen to result in the clock arriving as the latest or the earliest signal. Many of the receiver technologies appropriate for very-high-frequency operation do not use the incoming clock to sample the incoming data, which must be resampled and shifted to the local clock domain. Such receivers merely monitor changes in clock phase as the source clock drifts relative to the receiver's own clock, and thus do not care whether the clock transition is centered relative to the data transitions or at one extreme or another. Additionally, at these baud rates, receivers will often need to incorporate automatic deskewing circuits to function in real-world environments. For example, SCI protocols provide sync packets for dynamic skew compensation (see [B.1]). Dynamic skew compensation will need to be used in the circuit designer's systems if the cables and connectors used cannot assure meeting the 600 ps maximum skew specification.

The single-ended pairs that make up the differential signal are shown in figure 3-22. This picture shows the single ac receiver specification called t_{skew}. Here, t_{skew} is pictured as only one receiver differential input to another receiver differential input. It is the total allowable skew among parallel channels. The receiver must be able to correctly sample the logic state on all parallel channels when there is this much difference between the transitioning signals as they arrive at the inputs to the high-speed comparator. The t_{skew} includes that resulting from driver, interconnect, packaging, induced noise, etc. Differential signals V_{idm} and V_{idn} would be measured for the difference in delay at the receiver input, using the test circuit shown in figure 3-15.



NOTE— $V_{id}[m]$ and $V_{id}[n]$ are any two differential signals, including clock and flag, that are present at receiver inputs.

Figure 3-22 —t_{skew} diagram for receiver inputs



NOTE — This applies to all pairs of complementary single-ended signals.

Figure 3-23 —Skew1 diagram

Since LVDS receivers are expected to be integrated on VLSI parts, it is difficult to measure skew for difference in delay through a comparator. For this reason, the receiver skew is specified as a maximum tolerable timing difference (as observed on the receiver's inputs) for which the data will be sampled correctly. This specification implies that the internally sampled data values are accessible during testing.

When generating differential signals, two skews are important. Skew 1 is the skew between the high-to-low and low-to-high transitions of complementary single-ended channels (see figure 3-23). This skew can be the result of different propagation delays between complementary drivers, or different slew rates of the driver outputs. It is always measured at the V_{os} as defined in figure 3-7 for the single-ended signals. This skew creates EMR as discussed in 3.3.1.

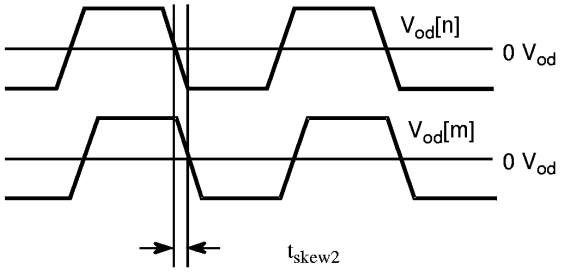
$$t_{\text{skew 1}} = \left|tp_{\text{HLA}} - tp_{\text{LHB}}\right| \quad or \quad \left|tp_{\text{HLB}} - tp_{\text{LHA}}\right| \tag{7}$$

where $tp_{\text{HLA/B}}$ and $tp_{\text{LHA/B}}$ are the propagation delays on outputs A and B for high to low and low to high.

Skew2 is the skew between any differential signals as they can be measured at the driver output. It results from circuit mismatches for complementary drivers and layout or packaging differences. As shown in figure 3-24, it is measured between parallel channels. Skew2 is always measured between any two parallel signals, at the 0 V differential point. If $tp_{\text{diff}}[i]$ is the differential delay of V_{od} through the LVDS driver *i*, and assuming that the (probably inaccessible) inputs to the driver are simultaneous, then

$$t_{\text{skew2}} = \left|tp_{\text{diff}}[m] - tp_{\text{diff}}[n]\right| \tag{8}$$

where *m* is any one of the parallel channels and *n* is any other channel.



Any two differential signals

Figure 3-24 —Skew2 diagram, measured between any parallel channels

The diagram in figure 3-25 shows a representative breakdown of a typical SCI signal path. The backplane could also represent a cable segment of the signal path. An estimate of how the skew budget could be allocated for each of the signal path elements up to the package input is given in table 3-4. The chip inside the package also has to tolerate the additional package-to-chip wiring skews.

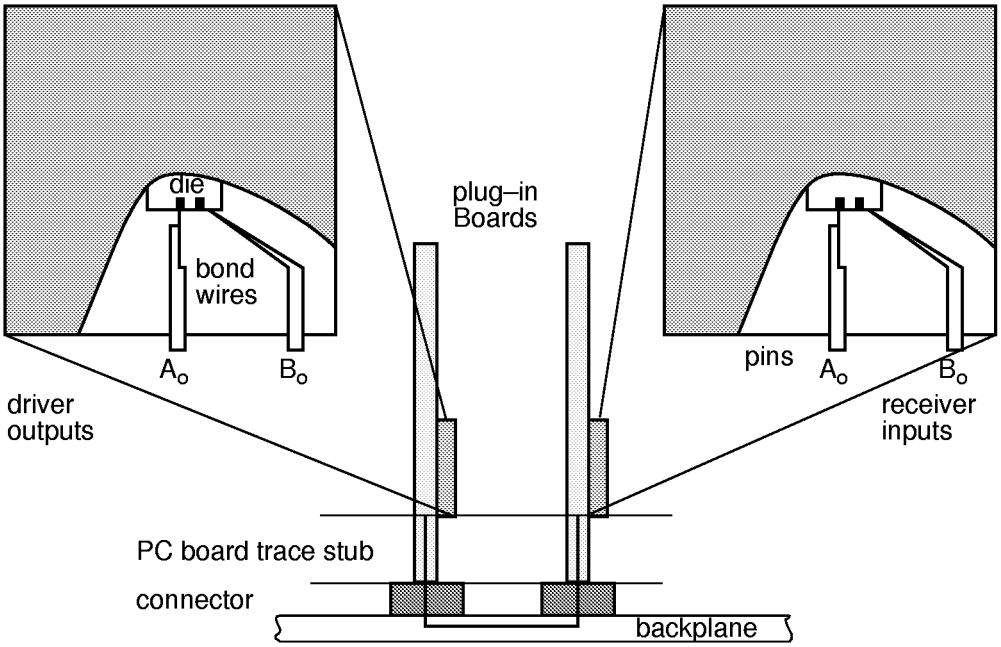


Figure 3-25 —Point-to-point connection segmented for skew allocation

Table 3-4 —Representative skew breakdown

Signal path	From	To	Skew max
Package	Internal signals	Package's driver pins	100 ps
PCB	Driver pins	Input of first connector	50 ps
Connector	Input of first connector	Output of first connector	25 ps
Media	Output of first connector	Input of second connector	350 ps
Connector	Input of second connector	Output of second connector	25 ps
PCB	Output of second connector	Receiver pins	50 ps
			Total = 600 ps

Annex A Bibliography

(Informative)

This document has been developed with point-to-point interconnects, such as the following standard, in mind:

[B1] IEEE Std 1596-1992, IEEE Standard for Scalable Coherent Interface (SCI) [ANSI].[2]

[2]This standard is currently in international balloting as an international Draft, where it bears the designation ISO/IEC DIS 13961. IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855–1331, USA.

Annex B SCI signal encoding

(Normative)

B.1 SCI symbol encoding

The SCI encoding specifies how packet types, packet lengths, and idle symbols are uniquely identified. Although the logical encoding is specified in terms of 16–bit symbols, the physical encoding layers support several data-path widths. Distinct physical encoding layers can be supported without changing the logical protocols, if they define how conversions between the physical and logical encodings are performed.

For 16-bit-wide links, one 16-bit SCI symbol is transmitted in each data-transfer period. In addition, a clock signal is needed to define symbol boundaries (the data should be stable when sampled), and a flag signal is used to locate the starting and ending symbols of packets.

The zero-to-one transition of the flag signal is used to mark the beginning of each packet, and the one-to-zero transition of the flag signal specifies the approaching end of each packet. The flag signal returns to zero for the final 4 symbols of send packets and for the final symbol of an echo packet as illustrated in figure B.1. A zero always accompanies the CRC of any packet, so the zero-to-one transition can be used to identify the start of the next packet (even when there is no idle symbol between them).

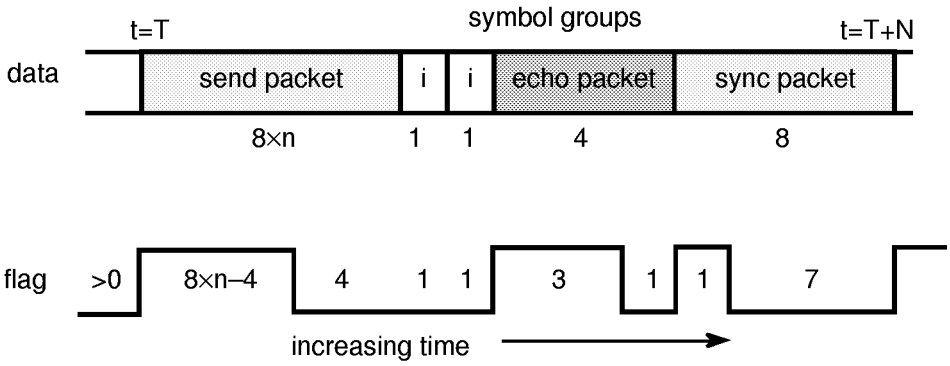


Figure B.1—Flag framing convention

The sync packets are used for initial synchronization of the physical receivers and for dynamic compensation of skew. Sync packets are always a pattern of one-bits the full width of the link, followed by zero-bits the full width of the link. Note that for P18 and wider encodings, the clock may have either a zero-to-one or a one-to-zero transition at the point in the sync packet where all other signals have a one-to-zero transition. (Packets may start at either clock transition in these wider encodings.) To simplify the design of the SCI interface hardware, the idle symbols are always 16 bits wide or the full width of the data path depending on which is larger.

It should be noted that the 1- and 16-bit encodings, which are specified in IEEE Std 1596–1992 and therefore not included in this annex, can also use this LVDS differential signaling standard.

B.2 Narrow parallel encoding

The 16-bit SCI symbols need not be sent in a single physical-clock-signal transition; multiple data-transfer cycles can be used. Encoding for use on physical links that are narrower than the 16-bit SCI logical symbol width use the polarity of the clock signal or extra transitions on the flag signal to mark the beginning of the logical symbol.

B.2.1 Parallel 8/10 (P10) encoding

On a byte-wide (8-data-bit) interface, half of an SCI symbol is sent in each of two data-transfer intervals. The clock signal changes before each subsymbol; the low and high clock-signal values identify the first and last subsymbol respectively. The flag line transitions occur at most once per symbol, as illustrated in figure B.2.

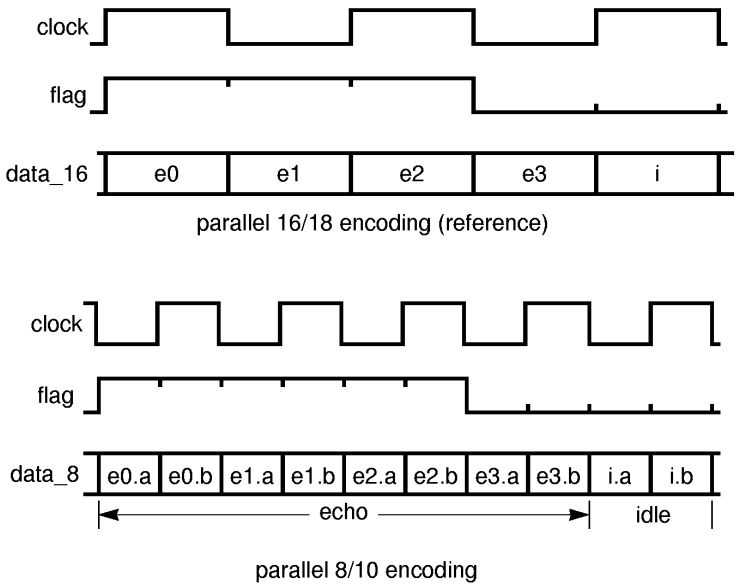


Figure B.2—Parallel 8/10 (P10) encoding

In this illustration, *e0.a* and *e0.b* bytes are the most- and least-significant bytes of the *e0* (echo-packet) symbol; *el.a* and *el.b* bytes are halves of the *el* symbol; *e2.a* and *e2.b* are halves of the *e2* symbol; *e3.a* and *e3.b* are halves of the *e3* symbol; *i.a* and *i.b* bytes are the most- and least-significant bytes of the *i* (idle) symbol.

The sync packet is 16 clock-periods long (8 symbols), to simplify conversions between P18 and P10 encodings, as illustrated in figure B.3.

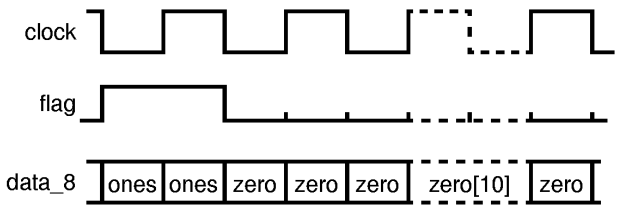


Figure B.3—Sync packet: parallel 8/10 (P10) encoding

B.2.2 Parallel 4/5 (P5) encoding

The 16-bit symbol may also be sent four bits at a time, using four subsymbols to form a logical SCI symbol. The clock and flag signals are combined, since the overhead of the extra signal is significant and 10-bit cables may then be used for two 5-bit links, one in each direction. The physical clock signal has a high-to-low transition at the start of each symbol; the flag value is derived by sampling the clock in the middle of each symbol period, as illustrated in figure B.4.

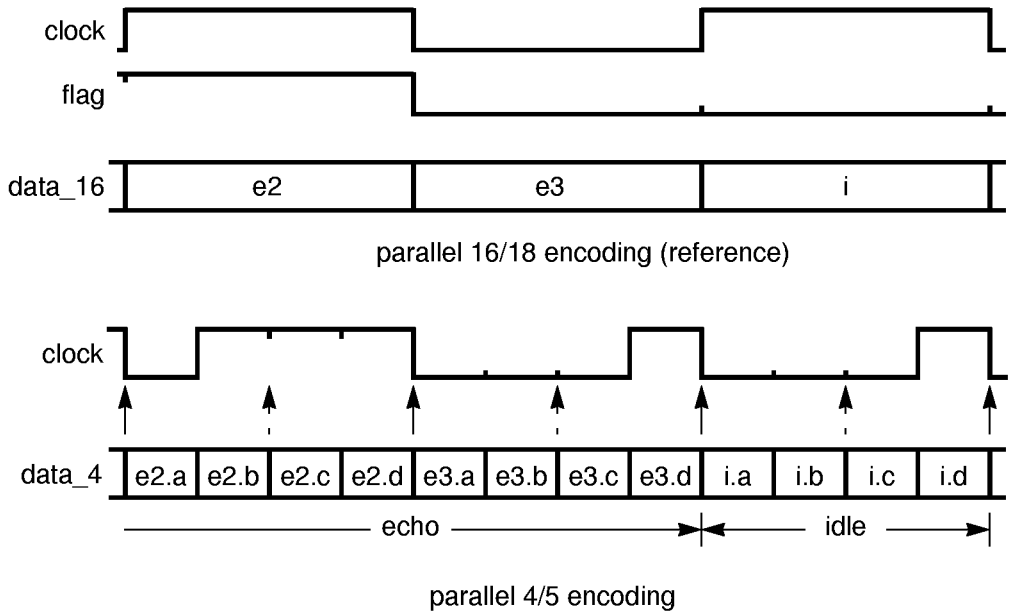


Figure B.4—Parallel 4/5 (P5) encoding

A high logical flag has a low-to-high clock-signal transition after the first subsymbol of each symbol. A low logical flag has a low-to-high clock-signal transition after the third subsymbol of each symbol.

The *e2.a*, *e2.b*, *e2.c*, and *e2.d* subsymbols are the most- through least-significant quarters of the *e2* (echo-packet) symbol; the *e3.a*, *e3.b*, *e3.c*, and *e3.d* subsymbols are the most- through least-significant quarters of the *e3* (echo-packet) symbol; the *i.a* and *i.b* subsymbols are the two most-significant quarters of the following idle symbol.

The sync packet is 16 clock-periods long (8 symbols), to simplify conversions between P18 and P5 encodings, as illustrated in figure B.5.

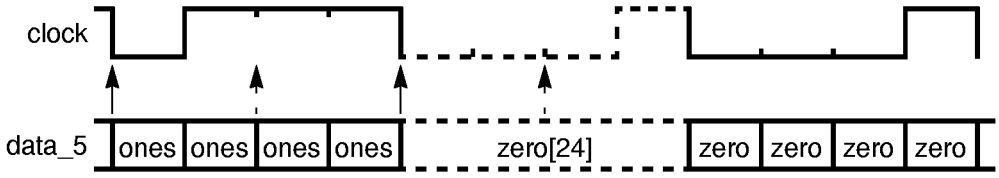


Figure B.5—Sync packet: 4/5 (P5) encoding

B.3 Wide parallel encoding

Encoding for links that are multiples of the 16-bit SCI logical symbol include the *clock* signal, provide an additional *sync* signal (to mark the beginning of a sync packet), and have one *flag* signal for each 16-bit data symbol. Transitions of the physical clock signal mark the boundaries of data-transfer intervals. The idle symbols are always the width of the link.

A sync packet consists of one data-transfer interval with ones on the *sync* signal, all *flag* signals and all data signals, followed by seven data-transfer intervals of zeroes on all these signals.

B.3.1 Parallel 32/36 (P36) encoding

On a 4-byte (32-bit) interface, two 16-bit SCI symbols are sent for each physical-clock-signal transition. There is a total of 36 signal pairs: clock, sync, and two sets of (flag + 16 data), as illustrated in figure B.6.

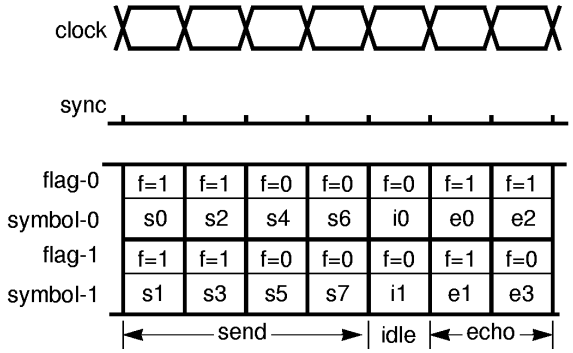


Figure B.6—Parallel 32/36 (P36) encoding

A sync packet, which remains 8 data periods in length, is illustrated in figure B.7.

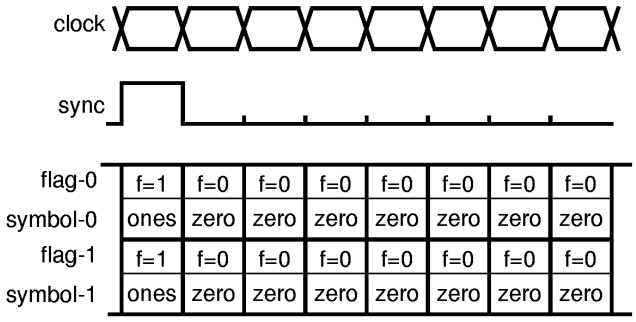


Figure B.7—Sync packet: 32/36 (P36) encoding

B.3.2 Parallel 64/70 (P70) encoding

On an 8-byte (64-bit) interface, four 16-bit SCI symbols are sent for each physical-clock-signal transition. There are a total of 70 signal pairs: clock, sync, and four sets of (flag + 16 data) signals, as illustrated in figure B.8.

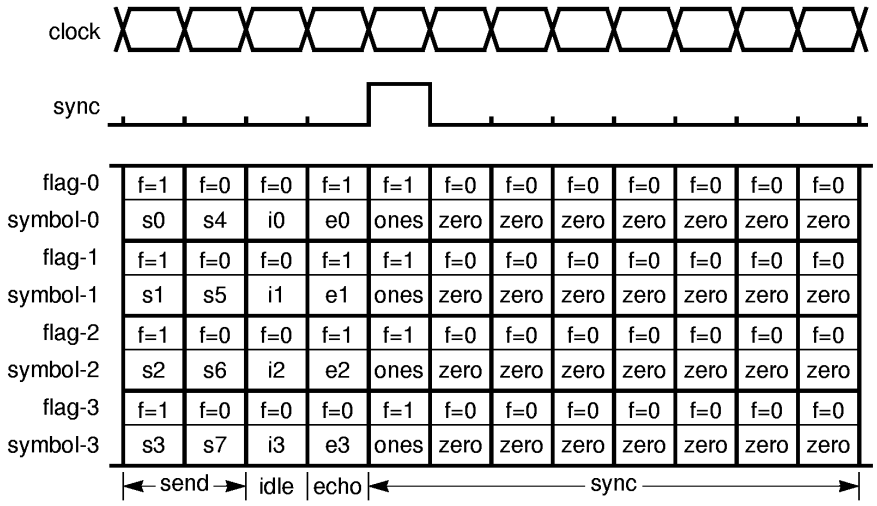


Figure B.8—Parallel 64/70 (P70) encoding

B.3.3 Parallel 128/138 (P138) encoding

On a 16-byte (128-bit) interface, eight 16-bit SCI symbols are sent for each physical-clock-signal transition. There are a total of 138 signal pairs: clock, sync, and eight sets of (flag + 16 data) signals, as illustrated in figure B.9.

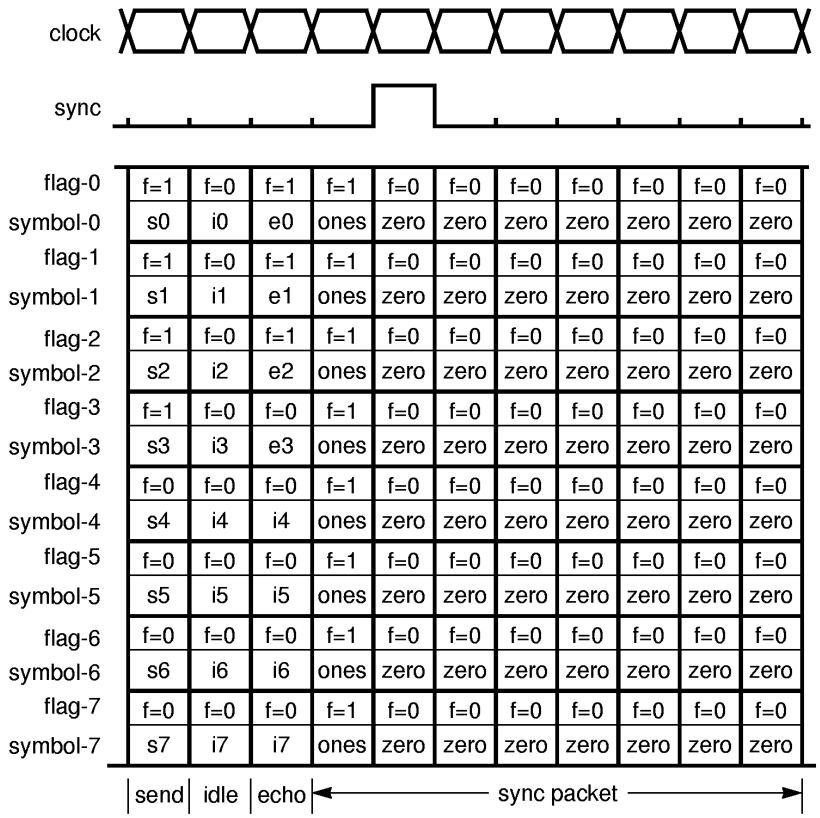


Figure B.9—Parallel 128/138 (P138) encoding

Annex C Driver and receiver models

(Informative)

C.1 Driver model

A driver design model is illustrated in figure C.1. This simplified model is only intended to give an idea of how to implement a near-constant-current differential driver. It is not necessarily a manufacturable or cost-effective design.

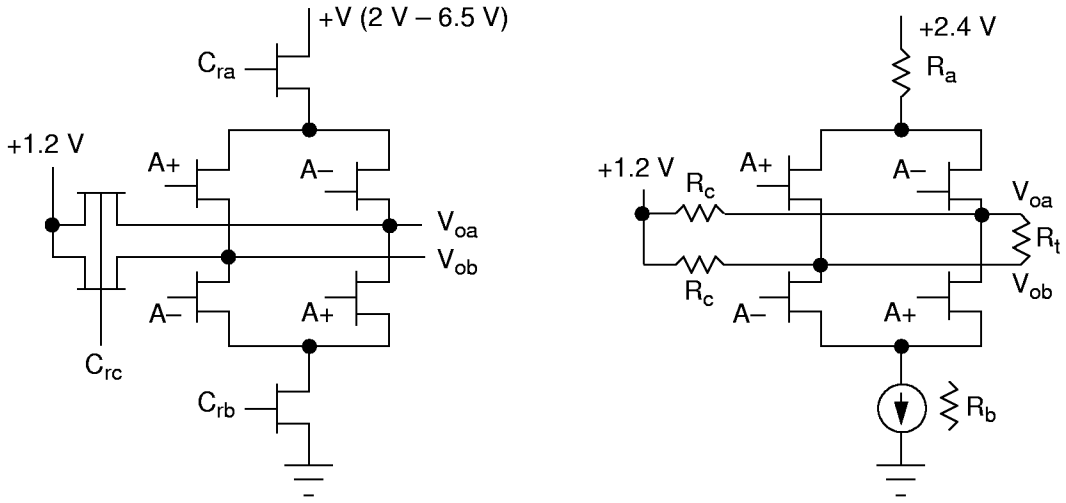


Figure C.1—Driver design model

C_{rb} is intended to operate as a current sink; however, at any particular operating condition it is equivalent to a resistance R_b. The voltage on C_{ra} is adjusted so that the attached transistor behaves like a voltage follower, providing the appearance of a resistance R_a connected to 2.4 V. The voltage on C_{rc} is adjusted so that these transistors behave like termination resistors of value R_c. R_t is the receiver termination.

Values are selected and/or adjusted so that R_a+R_{oa} and R_b+R_{ob} are closely matched, where the switching transistors have impedance of R_{oa} and R_{ob}. When so matched, the driver's output characteristics are illustrated in figure C.2.

Although constrained by the R_o (driver's output impedance) specification, the value of R_c may be significantly greater than the transmission line impedance of 50 Ω, to minimize driver power dissipation.

C.2 Receiver model

The receiver design model includes a terminating resistance (90–110 Ω), as illustrated in figure C.3.

The design of the receiver can be simplified by recognizing that the amplifier impedance need only be large compared to the receiver's termination impedance (100 Ω). Also, it may be easier to take advantage of the fact that SCI signals are always clocked; a combined amplifier/latch (i.e., sense amp) may be easier to build than an amplifier followed by an independent latch.

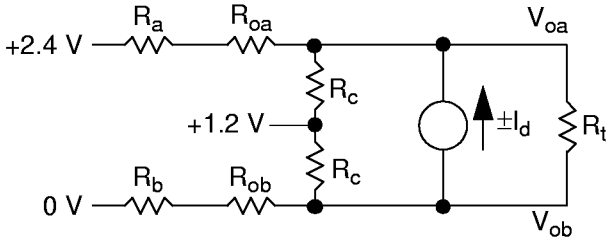


Figure C.2—Driver impedance characteristics

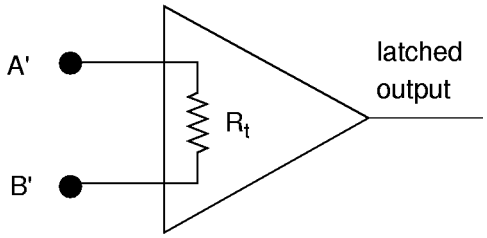


Figure C.3—Receiver design model

C.3 Signal transmission model

The signal-transmission model, including the driver, transmission line, and termination resistance within the receiver, is illustrated in figure C.4.

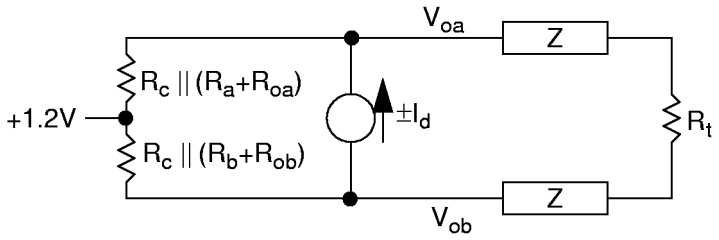


Figure C.4—Signal transmission model

APPENDIX D

April 25, 1997

Dear Valued Customer:

Enclosed is our first edition of *the LVDS Owner's Manual & Design Guide*. It can be ordered from our Customer Support Centers or through our Website (http://www.national.com) as literature# 550062-001. It can also be downloaded from our Website starting in June. There is a growing trend toward high speed differential serial buses, and this document is intended to help designers become familiar and comfortable with the benefits and use of this important new LVDS technology. The *Owner's Manual* contains:

Chapter 1: "Introduction to LVDS"
Explains how LVDS works and where the standard came from

Chapter 2: "LVDS Advantages"
Includes 3 case studies showing the total cost and performance of LVDS versus other technologies

Chapter 3: "Selecting an LVDS Device"
A selection guide

Chapter 4: "Designing with LVDS"
PCB and other design tips for creating high performance, low noise LVDS applications

Chapter 5: "Cables and Connectors"
Some general guidelines for selecting and using cables and connectors

Chapter 6: "LVDS Evaluation Boards"
A description of available eval boards and instructions for using the Generic LVDS Evaluation Board

Chapters 7 & 8: Reference Information & Index

I hope this and future versions of the *LVDS Owner's Manual* will be of use to you and your co-workers. If you have any questions, please contact your local sales representative or call the Interface Applications Hotline at 408/ 721-8500.

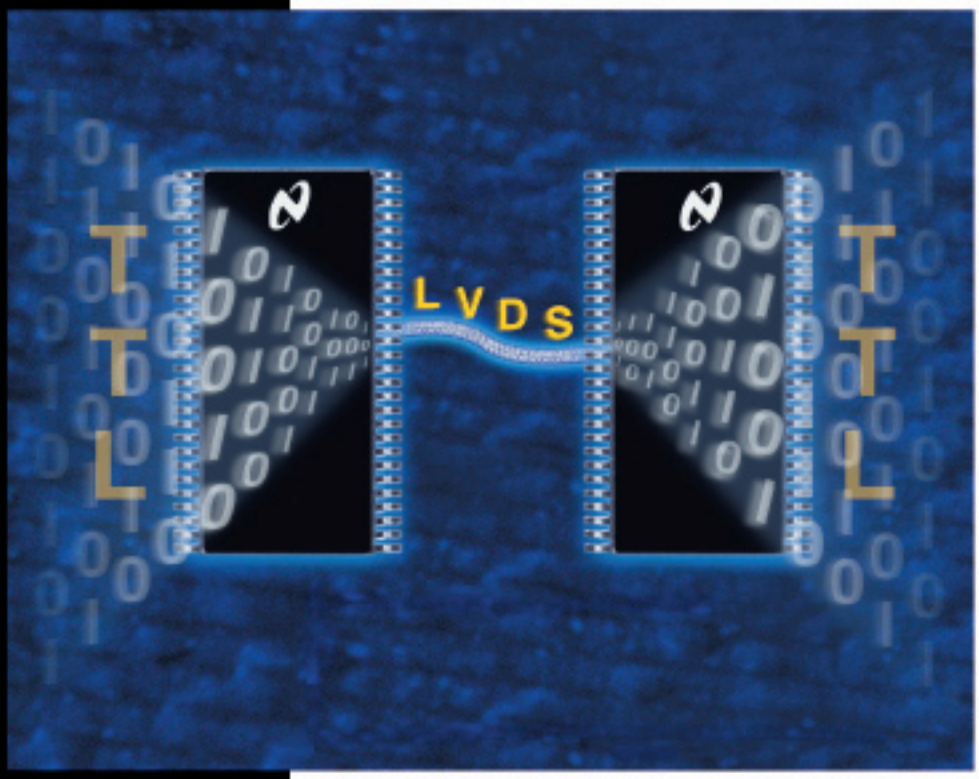
Sincerely,

Interface Signal Management Group
National Semiconductor

EMC EXHIBIT
1019

LVDS OWNER'S MANUAL

SPRING 1997



National Semiconductor

DESIGN GUIDE

Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) over two differential PCB traces or a balanced cable.

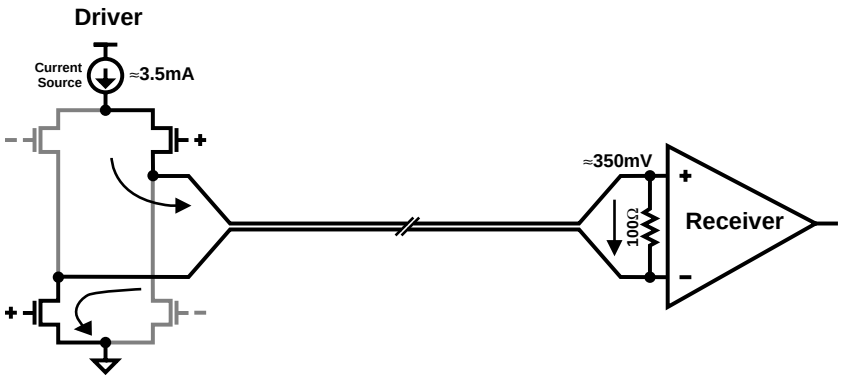
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics, and photorealistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board to board or box to box, however, requires an extremely high performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise, and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds of Megabits per second (Mbps). Its low swing and current mode driver outputs create low noise and provide a very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified diagram of LVDS driver and receiver connected via 100Ω controlled differential impedance media.

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives one of the differential pair lines. The receiver has high DC impedance (it does not source or sink DC current), so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that noise is coupled onto the two wires as common mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the *difference* between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current mode, very low — almost flat — power consumption across frequency is achieved since the power consumed by the load (3.5mA x 350mV ≈ 1.2mW) stays almost constant.

1.2.3 The LVDS Standards

Two key industry standards define LVDS: one from the ANSI/TIA/EIA (American National Standards Institute/Telecommunications Industry Association/Electronic Industries Association) and another from the IEEE (Institute for Electrical and Electronics Engineering).

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard

Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change in V_{OD}|		50	|mV|
ΔV_{OS}	|Change in V_{OS}|		50	|mV|
I_{SC}	|Short Circuit Current|		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)		30% of t_{ui}†	
I_{IN}	|Input Current|		20	|µA|
V_{TH}	|Threshold Voltage|		100	|mV|
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e bit width).

The ANSI/TIA/EIA standard does specify a recommended maximum data rate of 655Mbps and a theoretical maximum of 1.923Gbps based on a lossless medium. The standard also covers minimum media specifications, fail-safe operation of the receiver under fault conditions, and other configurations issues such as multi-receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the **IEEE 1596.3** standard. SCI-LVDS specifies also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB or cable thereby serving a broad range of applications.

1.2.4 A Quick Comparison

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2-5 V	±600-1,000 mV	±250-450 mV
Receiver Input Threshold	±200 mV	±200-300 mV	±100 mV
Data Rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter (Based on DS90C031/2)	RS-422	PECL	LVDS
Supply Current Quad Driver (no load, static)	60mA	32-65mA (Max.)	3.0mA
Prop. Delay of Driver	11ns (Max.)	4.5ns (Max.)	3.0ns (Max.)
Prop. Delay of Receiver	30ns (Max.)	7.0ns (Max.)	5.0ns (Max.)
Supply Current Quad Receiver (no load, static)	23mA (Max.)	40mA (Max.)	10mA (Max.)
Skew (Driver or Receiver)	N/A	500ps	400ps

The chart above compares LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are 1/10 of traditional TTL/CMOS and RS-422 levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate high speed signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions.

To prevent reflections, LVDS requires a terminating resistor of 100Ω ± 20Ω that is matched to the actual cable or PCB traces. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input . With this termination, an LVDS driver (DS90C031) can drive a twisted pair wire (e.g. SCSI cable) over 10m at speeds in excess of 155.5Mbps (77.7MHz). The real limitation on speed is two fold: 1) how fast TTL data can be delivered to the driver, 2) bandwidth performance of the selected media (cable). In the case of LVDS drivers like the DS90C031, its speed is limited by how fast the TTL data can be delivered to the driver. (National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.)

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ωs across the receiver input.

1.2.6 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS. Similarly, LVDS devices require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its CMOS current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (<50mA total for driver+receiver at 100MHz). Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

1.2.7 Fail-Safe Feature

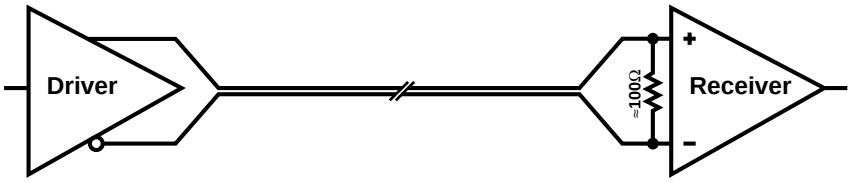
To help ensure reliability, LVDS receivers have a fail-safe feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, or terminated receiver inputs.

If the driver loses power, is disabled or is removed from the line, while the receiver stays powered on with inputs terminated, the receiver output remains in a known state with the fail-safe feature.

If LVDS receivers did not have the fail-safe feature and one of the fault conditions occurred, any external noise above the receiver thresholds could trigger the output and cause an error. A receiver without fail-safe could even go into oscillation under certain fault conditions. The fail-safe features ensures that the receiver output will be a HIGH — rather than an unknown state — under fault conditions.

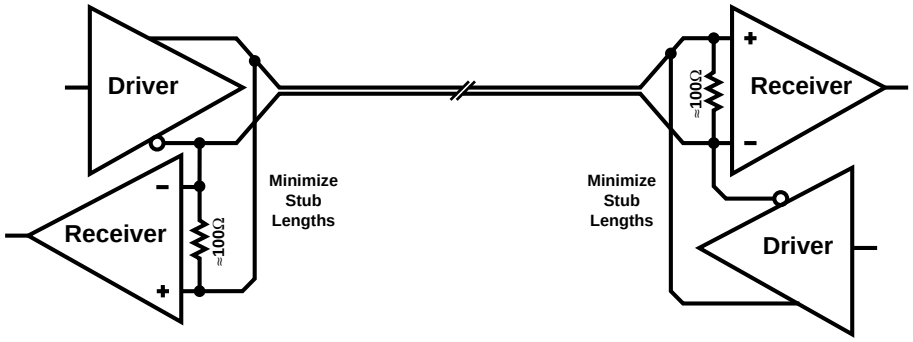
With the fault conditions accommodated internal to the receiver, designers do not need to include the external biasing resistors required by other technologies. This LVDS advantage saves valuable board space, cost, and design headaches.

1.2.8 LVDS Configurations

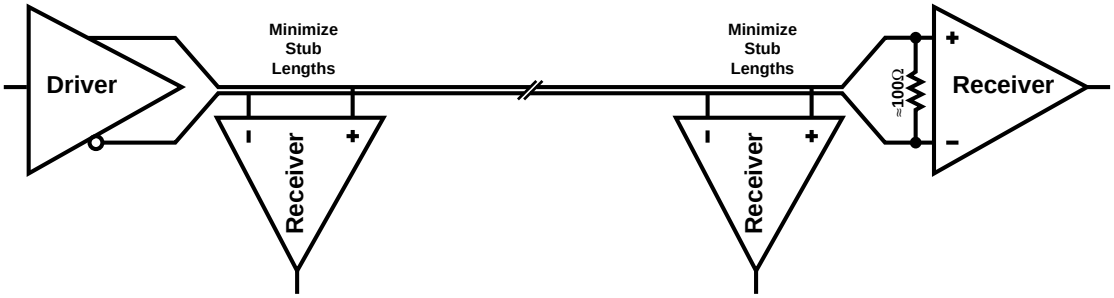


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m).



Bi-directional half-duplex configuration.



Multidrop configuration.

A multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Dedicated point-to-point links are still the preferred solution. LVDS has many advantages that make it likely to become the next data transmission standard for data rates at and above 100Mbps for distances around 10m or less. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the RS-232, RS-422, and RS-485 standards.

1.3.0 SAVE MONEY TOO

LVDS can save money in several important ways:

1) National's LVDS solutions are inexpensive CMOS implementations.

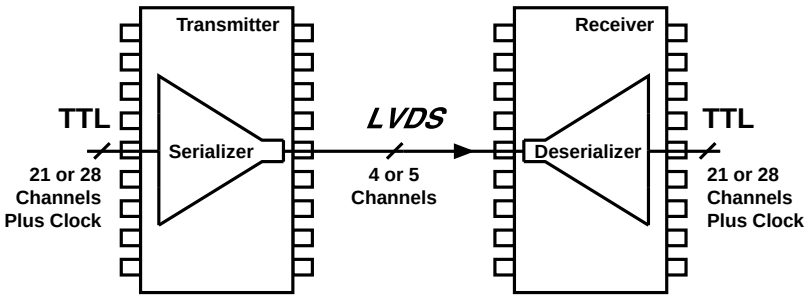
2) High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors.

3) LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.

4) LVDS is a low noise producing, noise tolerant technology power supply and EMI noise headaches are greatly minimized.

5) LVDS transceivers are relatively inexpensive and can also be integrated around digital cores.

6) Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or muxed into a single LVDS channel, reducing board, connector, and cable costs. National's family of Channel Link devices do just that. A channel link transmitter takes 21 or 28 bits of TTL data and converts it to 4 or 5 LVDS channels. These 4 or 5 channels of LVDS can then be routed across controlled impedance PCB traces or cable to the receiver which converts the data back to TTL.



National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and then back to TTL.

The conversion of a wide TTL bus to a few LVDS channels using Channel Link can substantially lower the power required to move the data, reduce noise and EMI concerns, and dramatically cut the size and number of PCB layers, connector pins, and cable conductors. In fact in most cases, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV031/DS90LV032 quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and transceivers.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) LVDS interface devices. These parts make it practical for portable computers to take advantage of the same high screen resolutions used in CRT-based desktop PCs.

Another more generalized use of LVDS is in the National Channel Link family which can take 21 or 28-bits of TTL data and convert it to 3 or 4 channels of LVDS plus clock. These devices provide fast data pipes (up to 1.84Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost high speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

LVDS Advantages

Chapter 2

2.0.0 LVDS ADVANTAGES

2.1.0 LVDS ELECTRICAL CHARACTERISTICS

LVDS current-mode, low-swing outputs mean that LVDS can drive at high speeds (up to several hundred Mbps over short distances). If high speed differential design techniques are used, signal noise and electromagnetic interference (EMI) can also be reduced with LVDS because of:

1) The low output voltage swing (≈350mV)

2) Relatively slow edge rates, dV/dt ≈ 0.350V/0.5ns = 0.7V/ns

3) Differential (odd mode operation) so magnetic fields tend to cancel

4) "Soft" output corner transitions

5) Minimum I_{CC} spikes due to low current mode operation

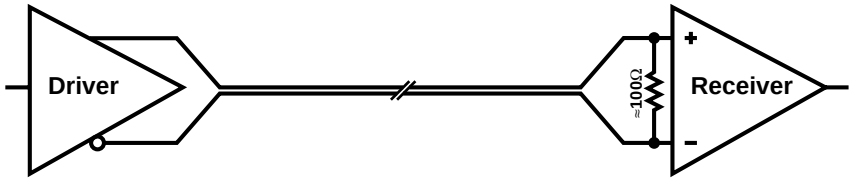
LVDS can be designed using CMOS processes, allowing LVDS to be integrated with standard ASICs. LVDS can be used in commercial, industrial, and even military temperature ranges and operate from power supplies down to 2 volts. LVDS uses common copper PCB traces and readily available cables and connectors as transmission media, unlike fiber optics.

Presently the major limitations of LVDS are its point-to-point nature (as opposed to multipoint) and short transmission distance (10-15m), where other technologies must presently be used.

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1Gbps	+	+	+	-	-	-
Very low skew	+	+	+	-	+	-
Low dynamic power	+	-	+	-	-	-
Cost effective	+	-	-	+	+	+
Low noise/EMI	+	+	+	-	-	-
Single power supply/reference	+	-	+	+	-	+
Migration path to low voltage	+	-	+	-	+	+
Simple termination	+	-	-	+	-	+
Wide common mode range	-	+	+	+	-	-
Process independent	+	-	+	+	+	+
Allows integration w/digital	+	-	-	-	+	+
Cable breakage/splicing issues	+	+	-	+	+	+
Long distance transmission	-	+	+	+	-	-
Industrial temp/voltage range	+	+	+	+	+	+

2.2.0 LVDS DRIVERS & RECEIVERS

The most basic LVDS devices are the driver and receiver. These translate TTL to LVDS and back to TTL.

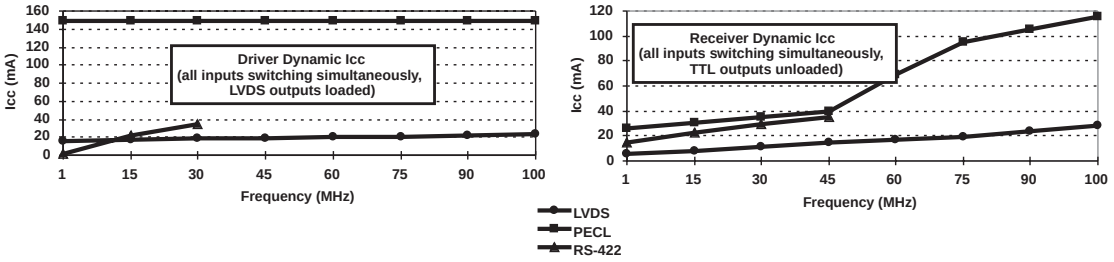


LVDS drivers and receivers convert TTL to LVDS and back to TTL.

Drivers and receivers transmit high speed data across distances up to 10m at very low power, noise, and cost.

Parameter	LVDS	PECL	Optics	RS-422	GTL	TTL
Output voltage swing	±350mV	±800mV	n/a	±2-5V	1.2V	2.4-5V
Receiver threshold	±100mV	±200mV	n/a	±200mV	100mV	1.2V
Speed (Mbps)	>400	>400	1000	<30	<200	<100
Dynamic power	Low	High	Low	Low	High	High
Noise	Low	Low	Low	Low	Med	High
Cost	Low	High	High	Low	Low	Low

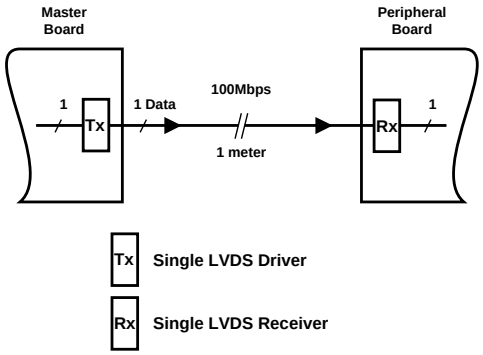
The table above summarizes that only LVDS can deliver the high speed, ultra-low power, and low cost without compromise. PECL and ECL are expensive and consume too much power. TTL/CMOS is cheap, but is noisy and burns a lot of power at high speeds. Fiber optics are expensive and have cables and connectors which are hard to manage.



I_{CC} vs. Frequency for 5V DS90C031/032 LVDS, 41LG/LF PECL, and 26C31/32 RS-422 devices.

2.2.1 100Mbps Serial Interconnect

LVDS drivers and receivers are generally used to create serial or pseudo-serial point-to-point interconnects from 1Mbps to 400Mbps per channel. The following example summarizes the total performance and cost advantages of using LVDS over PECL or TTL for a serial 100Mbps 1 meter point-to-point link. Significantly higher data rates can be achieved for LVDS and PECL.



100Mbps Board-to-Board Link

100Mbps Serial Bitstream

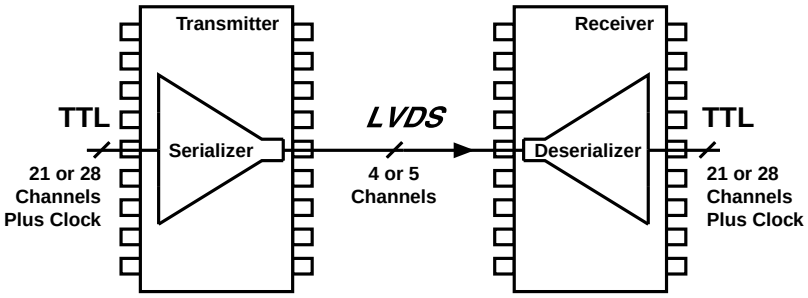
Performance Estimate				
Characteristic	**Parameter**	**LVDS**	**TTL**	**PECL**
Speed	Application Data Rate (Mbps)	100	100	100
	Max Capability per Channel (Mbps)	200	100	200
Power Consumption	Dynamic (mA) (@ 50MHz)	Low	High	Medium
	Static (mA)	8	10	48
Noise	Low EMI	+++	- - -	++
	Low Bounce	+++	- - -	++
Relative System Cost	**Total**	**4.05**	**3.30**	**6.10**
Cost Estimate				
Subsystem	**Parameter**	**LVDS**	**TTL**	**PECL**
General	Single-Ended or Differential	Differential	Single-Ended	Differential
	TTL Bus Width	1	1	1
	TTL Bus Speed (MHz)	50	50	50
	# Master Boards	1	1	1
	# Slave Boards	1	1	1
Transceivers	Description	DS90LV017/018	74LVT125	10ELT20/21
	# Drivers/Board (Master Board)	1	1	1
	# Rec/Board (Peripheral Board)	1	1	1
	Unit Cost	1.00	0.60	2.00
	Silicon Cost per Board	2.00	1.20	4.00
Termination	Voltage	None	None	None
	# Termination Regulators	0	0	0
	Unit Cost	0.00	0.00	0
	# Termination Resistors	1	2	2
	Unit Cost	0.05	0.05	0.05
	# Termination Capacitors	0	0	0
	Unit Cost	0.00	0.00	0.00
	Total Termination Cost	0.05	0.10	0.10
Transmission Medium	Cable Type	2 Pair CAT3	2 Pair CAT3	2 Pair CAT3
	Distance	1m	1m	1m
	#Conductors	2	2	2
	#Cables	1	1	1
	Connector Type	4-pin Wire to Board	4-pin Wire to Board	4-pin Wire to Board
	Unit Cable+Connector Assembly Cost	2.00	2.00	2.00
	Total Media Cost	2.00	2.00	2.00
Total Relative System Cost		**4.05**	**3.30**	**6.10**

Total Performance and Cost Estimates

The preceding example shows that LVDS provides a high speed link with minimal noise, power, and cost. LVDS also creates an easy migration path to higher speeds, lower supply voltages, and higher integration that the other do not.

2.3.0 LVDS CHANNEL LINK SERIALIZERS

The speed of the LVDS line drivers and receivers is limited by how fast the TTL signals can be switched. Therefore, National has introduced a family of Channel Link serializers and deserializers. Instead of using one LVDS channel for every TTL channel, the Channel Link devices send multiple TTL channels through every LVDS channel thereby matching the speed of LVDS to that of TTL.



National's Channel Link serializers/deserializers can dramatically reduce the size (and cost) of cables and connectors.

Using fewer channels to convey data also means power and noise can be lower. The biggest advantage, however, is the significant reduction of cable and connector size. Since cables and connectors are usually quite expensive compared to silicon, dramatic cost savings can be achieved. Channel Link chipsets reduce cable size by up to 80%, reducing cable costs by as much as 50%. Plus, smaller cables are more flexible and user-friendly.

LVDS Channel Link serializer/deserializer devices take the inherent high speed low power, noise, and cost advantages of LVDS and capitalize on the slow speed of TTL to generate significant benefits. For a small increase in silicon cost, Channel Link products can dramatically reduce total system costs and improve total system performance. Therefore, the total system should be evaluated if the true advantages are to be quantified. The following sections summarizes the cost and performance benefits of using Channel Link devices.

2.2.1 1Gbps 16-bit Interconnect

National's Channel Link serializers/deserializers take the benefits of LVDS (high speed and low power, noise, and cost) and add serialization to further reduce cable, connector, and PCB size and cost. Channel Link is a great solution for high speed data bus extension when the the overhead of protocols is not desired. The following example compares the total performance and cost of moving a 16-bit 66MHz bus across 1 meter of cable using the 3V 66MHz 21-bit DS90CR215/216 Channel Link devices versus other solutions.

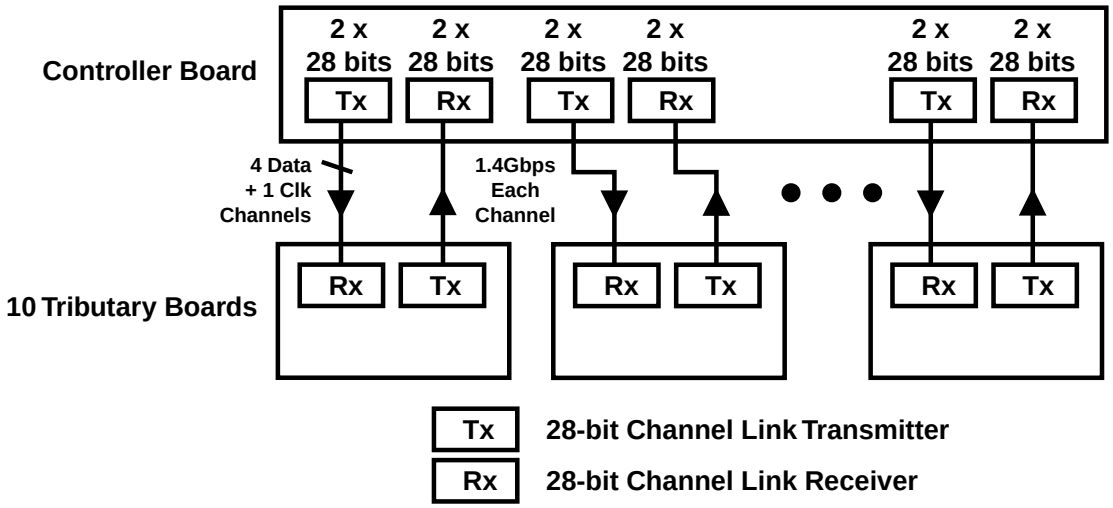
16-Bit Cable Interconnect

Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1056	1056	1056	1056	1056
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 66MHz)	180	300	500	300	?
	Static (mA) (Outputs Disabled)	0.02 (Power Dn)	1	50	50	135
Noise	Low EMI	+++	- - -	- -	+	+++
	Low Bounce	+++	- - -	- -	++	+++
Ergonomics	Compact System Size	+++	- -	- -	- - -	+++
	Compact Transmission Medium Size	+++	-	+	+	+++
	Low Weight	+++	-	-	-	+++
Relative System Cost	**Total**	**25.50**	**55.80**	**58.80**	**71.80**	**77.60**
Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Differential	Differential ECL
	TTL Bus Width	16	16	16	16	16
	TTL Bus Speed (MHz)	66	66	66	66	66
	Multiplexed Scheme?	Yes	No	No	No	Yes
	# Master Boards	1	1	1	1	1
	# Slave Boards	1	1	1	1	1
Transceivers	Description	3V 21:4 Channel Link	ALVT 16-Bit	GTL 18-Bit	9-Bit Translators	Fibre Channel
	# Drivers/Board (Master Board)	1	1	1	2	1
	# Rec/Board (Peripheral Board)	1	1	1	2	1
	Unit Cost	5.00	2.50	3.50	5.00	20.00
	Silicon Cost per Board	10.00	5.00	7.00	20.00	40.00
PC Board	Layers	4	12	12	12	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	15.00	15.00	15.00	15.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	# Termination Regulators	0	0	1	1	1
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	# Termination Resistors	10	16	16	16	32
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	# Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	0.80	1.80	1.80	2.60
Transmission Medium	Cable Type	SCSI2 CAT3 Cable	Shielded Flat Cable	Shielded Flat Cable	SCSI2 CAT3 Cable	CAT5 Cable
	Distance	2m	2m	2m	2m	2m
	#Data+Clock Conductors	8	17	17	34	2
	#Power+Ground Conductors	4	10	10	15	2
	#Cables	1	1	1	1	1
	Connector Type	0.050 D - 20	D - 37	D - 37	0.050 D - 50	DB-9
	Unit Cable+Connector Assembly Cost	20.00	30.00	30.00	30.00	15.00
	Total Media Cost	15.00	30.00	30.00	30.00	15.00
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.3	1.2	1.2	1.2
	Total Add'l Power Supply Cost	0.00	5.00	5.00	5.00	5.00
Total Relative System Cost		**25.50**	**55.80**	**58.80**	**71.80**	**77.60**

Total Performance and Cost Estimates

2.2.2 1.4Gbps 56-Bit Backplane

In some large datacom and telecom systems, it is necessary to construct a very large, high speed backplane. There is generally an inverse relationship between the size of a backplane and its maximum speed. In other words, if you try to make a backplane too large, the heavy loading will severely hamper backplane speed and make power and noise a big problem. Therefore, connecting or extending smaller backplanes via a high speed cable interconnect is often the only solution. The previous examples illustrates how Channel Link may be used to accomplish this over cable. The cost benefits of using Channel Link to shrink cable and connector costs are clear. What would happen, however, if Channel Link were used to form or extend a backplane using a PCB as the medium. The following examples shows how Channel Link can reduce the size and number of layers of the printed circuit board transmission medium in the same way as Channel Link reduces the size and cost of cables.



1.4Gbps Backplane Using Point-to-Point Channel Links

56-Bit Blackplane

Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1400	1400	1400	1400	1400
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 50MHz)	2600	10000	6000	16000	?
(Loaded Tx/Rx's only)	Static (mA)	0.4 (Power on)	40	1840	3402	3818
Noise	Low EMI	+++	---	+	+	++
	Low Bounce	+++	---	+	+	++
Ergonomics	Compact System Size	++	+	+	+	++
	Compact Transmission Medium Size	++	-	+	+	++
	Fans?	No	No	No	Yes	Yes
	Low Weight	+++	-	-	-	+++
Relative System	**Cost Per Board**	**51.05**	**66.12**	**75.04**	**191.04**	**574.22**
	Total	**510.50**	**661.20**	**750.40**	**1910.40**	**5742.20**
Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Differential
	TTL Bus Width	56	56	56	56	56
	TTL Bus Speed (MHz)	50	50	50	50	50
	Multiplexed Scheme?	Yes	No	No	No	Yes
	Number Tributary Boards	10	10	10	10	10
	Number Channels in Link	10	56	56	56	14
	Number Conductors (Data)	20	56	56	56	28
	Number Conductors (CLK)	1	1	1	1	1
Transceivers	Description	28:5 Channel Link	LVT 16-Bit	GTL 18-Bit	9-Bit	Fibre Channel
	# Transceivers/Board (Trib Board)	4	4	4	14	14
	# Transceivers/Board (Ctrlr Board)	4	4	4	14	14
	Unit Cost	6.00	2.50	3.50	5.00	20.00
	Silicon Cost per Board	48.00	20.00	28.00	140.00	560.00
PC Board	Layers	12	26	26	26	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	100.00	100.00	150.00	50.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	Number Termination Regulators	0	0	14	14	14
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	Number Termination Resistors	10	224	128	128	14
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	Number Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	11.20	20.40	20.40	14.70
Transmission Medium	Type	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane
	Distance	<1m	<1m	<1m	<1m	<1m
	Layers	12	26	26	26	12
	Size (Normalized)	1	1	1	1	1
	Number Media	1	1	1	1	1
	Additional Media Cost	0.00	200.00	200.00	200.00	0.00
	Total Add'l Trans. Media Cost	0.00	200.00	200.00	200.00	0.00
Connectors	Connector Type	Header	VME	VME	VME	Header
	Number Pins (Data+ CLK)	21	57	57	57	29
	Number Pins (Power/GND)	5	38	38	7	7
	Total Connector Pins	26	96	96	64	36
	Number Connector Pairs	1	1	1	1	1
	Cost of Pair	3.00	10.00	10.00	8.00	3.75
	Connector Cost per Board	3.00	10.00	10.00	8.00	3.75
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.5	1.5	1.7	1.4
	Total Add'l Power Supply Cost	0.00	50.00	50.00	60.00	40.00
Total Relative System Cost Per Board		**51.05**	**66.12**	**75.04**	**191.04**	**574.22**
Total Relative System Cost		**510.50**	**661.20**	**750.40**	**1910.40**	**5742.20**

Total Performance and Cost Estimates

Selecting an LVDS Device

Chapter 3

3.0.0 SELECTING AN LVDS DEVICE

3.1.0 GENERAL

National is continually expanding its portfolio of LVDS devices. The devices listed below are current at the time this book goes to press. For the latest list of LVDS devices, contact your local National Semiconductor representative (listed on the back cover of this book). By far the best way to acquire the latest LVDS datasheet is through National's Website: http://www.national.com. The Web is constantly updated with new documents, whereas databooks and datasheets are printed infrequently. Applications questions should be directed to your local National Semiconductor representative or to the US National Interface Hotline: 1-408-721-8500 (8am to 5pm PST).

3.2.0 LVDS LINE DRIVERS & RECEIVERS

LVDS line drivers and receivers are used to convey information over PCB trace or cable if, (1) you only have a few channels of information to transmit, or (2) your data is already serialized. The table below summarizes National's LVDS line drivers and receivers.

LVDS Driver/Receiver Solutions

Order Number	Number of Drivers	Number of Receivers	Power Supply	Temp Range	Data Rate	Approx. I_{CC} @ 1Mbps	Max I_{CC} Disabled	Max Driver Prop Delay	Max Driver Channel Skew	Max Receiver Prop Delay	Max Receiver Channel Skew	Package	Comments	Eval Board Lit #
DS90C031TM	4	0	5	Ind	>155Mbps	21	4	3.5	1.0	—	—	16 SOIC	Ganged Enable	550061-001
DS90C031E-QML	4	0	5	Mil	>100Mbps	25	10	5.0	3.0	—	—	20 LCC	Military -883	550061-001
DS90C032TM	0	4	5	Ind	>155Mbps	11	10	—	—	6.0	1.5	16 SOIC	Ganged Enable	550061-001
DS90C032E-QML	0	4	5	Mil	>100Mbps	11	11	—	—	8.0	3.0	20 LCC	Military -883	550061-001
DS36C200M	2	2	5	Com	>155Mbps	17	10	5.5	—	9.0	—	16 SOIC	1394 Link	–
DS90C401M	2	0	5	Com	>155Mbps	21	6.5	3.5	1.0	—	—	8 SOIC		550061-001
DS90C402M	0	2	5	Com	>155Mbps	11	10	—	—	6.0	1.5	8 SOIC		550061-001
DS90LV031TM	4	0	3.3	Ind	>100Mbps	19	3	5.0	1.8	—	—	16 SOIC	Ganged Enable	550061-001
DS90LV032TM	0	4	3.3	Ind	>100Mbps	19	15	—	—	6.5	1.7	16 SOIC	Ganged Enable	550061-001
DS90LV017M	1	0	3.3	Com	>100Mbps	4	7	6.0	—	—	—	8 SOIC		550061-001
DS90LV027M	2	0	3.3	Com	>100Mbps	TBD	7	6.0	TBD	—	—	8 SOIC		550061-001
DS90LV018M	0	1	3.3	Com	>200Mbps	TBD	TBD	—	—	TBD	—	8 SOIC	Fall 1997	550061-001
DS90LV028M	0	2	3.3	Com	>200Mbps	TBD	TBD	—	—	TBD	TBD	8 SOIC	Fall 1997	550061-001
DS90LV019TM	1	1	3.3/5	Ind	>155Mbps	TBD	6	3.5	—	6.0	—	14 SOIC	Summer 1997	–
DS90LV031ATM	4	0	3.3	Ind	400Mbps	3.5	5	2.5	0.5	—	—	16 SOIC	Fall 1997	550061-001
DS90LV032ATM	0	4	3.3	Ind	400Mbps	1.5	15	—	—	3.5	0.5	16 SOIC	Fall 1997	550061-001

Note: When using drivers/receivers to transmit clock signals, multiply the clock frequency by 2 to get data rate.
Thus, a 50 MHz clock has 2-bits of information (a high bit and a low bit) for every clock period resulting in a 100 Mbps signal.

3.3.0 LVDS CHANNEL LINK SERIALIZERS/DESERIALIZERS

If you have a wide TTL bus that you wish to transmit, use one of National's Channel Link devices. Channel Link will serialize your data for you, saving you money on cables and connectors and helping you avoid complex skew problems associated with a completely parallel solution. The next table summarizes National's Channel Link devices.

Channel Link Solutions

Order Number	Mux/ Demux Ratio	Transmitter/ Receiver	Power Supply	Clock Frequency	Max Throughput	Package	Eval Board Order #
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	48TSSOP	–
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	48TSSOP	–
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	48TSSOP	CLINK5V21BT-66
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	48TSSOP	CLINK5V21BT-66
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	48TSSOP	CLINK3V21BT-66
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP	CLINK3V21BT-66
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	56TSSOP	–
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	56TSSOP	–
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	56TSSOP	CLINK5V28BT-66
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	56TSSOP	CLINK5V28BT-66
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	56TSSOP	CLINK3V28BT-66
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP	CLINK3V28BT-66

LVDS Channel Link Latency

Order Number	Mux/Demux Ratio	Transmitter /Receiver	Power Supply	Clock Frequency	Max Throughput	Latency	TCCD/RCCD Clock Delay (ns) Min	Typ	Max
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	TCCD †	5.0	7.5	10.7
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	1 Clock Period + RCCD	7.6	9.0	11.9
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	TCCD †	3.5	5.0	8.5
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	1 Clock Period + RCCD	6.4	8.0	10.7
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	1 Clock Period + TCCD †	TBD	5.3	TBD
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	2 Clock Periods + RCCD	TBD	6.9	TBD
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	TCCD †	5.0	7.5	10.7
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	1 Clock Period + RCCD	7.6	9.0	11.9
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	TCCD †	3.5	5.0	8.5
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	1 Clock Period + RCCD	6.4	8.0	10.7
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	1 Clock Period + TCCD †	TBD	5.3	TBD
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	2 Clock Periods + RCCD	TBD	6.9	TBD

† Substitute TCCD = (1/14 clock period + ≈3ns) for a more accurate transmitter latency calculation.
Contact National regarding the latency of future Channel Link devices not listed here.

3.4.0 LVDS FPD-LINK

Use National's FPD Link to convey graphics data from your PC/notebook motherboard to your flat panel displays. The next table summarizes National's FPD Link devices.

LVDS Flat Panel Display Link FPD-Link Solutions

Order Number	Color	Transmitter /Receiver	Power Supply	Max Clock Frequency	Clock Edge Strobe	Package	Eval Board Order #
DS90CF561MTD	18-bit	Transmitter	5	40MHz	Falling	48TSSOP	–
DS90CR561MTD	18-bit	Transmitter	5	40MHz	Rising	48TSSOP	–
DS90CF562MTD	18-bit	Receiver	5	40MHz	Falling	48TSSOP	–
DS90CR562MTD	18-bit	Receiver	5	40MHz	Rising	48TSSOP	–
DS90CF581MTD	24-bit	Transmitter	5	40MHz	Falling	56TSSOP	–
DS90CR581MTD	24-bit	Transmitter	5	40MHz	Rising	56TSSOP	–
DS90CF582MTD	24-bit	Receiver	5	40MHz	Falling	56TSSOP	–
DS90CR582MTD	24-bit	Receiver	5	40MHz	Rising	56TSSOP	–
DS90CF583MTD	24-bit	Transmitter	5	65MHz	Falling	56TSSOP	FLINK5V8BT-65
DS90CR583MTD	24-bit	Transmitter	5	65MHz	Rising	56TSSOP	Use 'CF583 Board
DS90CF563MTD	18-bit	Transmitter	5	65MHz	Falling	48TSSOP	FLINK5V6BT-65
DS90CR563MTD	18-bit	Transmitter	5	65MHz	Rising	48TSSOP	Use 'CF563 Board
DS90CF564MTD	18-bit	Receiver	5	65MHz	Falling	48TSSOP	FLINK5V6BT-65
DS90CR564MTD	18-bit	Receiver	5	65MHz	Rising	48TSSOP	Use 'CF564 Board
DS90CF584MTD	24-bit	Receiver	5	65MHz	Falling	56TSSOP	FLINK5V8BT-65
DS90CR584MTD	24-bit	Receiver	5	65MHz	Rising	56TSSOP	Use 'CF584 Board
DS90C363MTD	18-bit	Transmitter	3.3	65MHz	Programmable	48TSSOP	FLINK3V8BT-65
DS90CF363MTD	18-bit	Transmitter	3.3	65MHz	Falling	48TSSOP	Use 'C363 Board
DS90C383MTD	24-bit	Transmitter	3.3	65MHz	Programmable	56TSSOP	FLINK3V8BT-65
DS90CF383MTD	24-bit	Transmitter	3.3	65MHz	Falling	56TSSOP	Use 'C383 Board
DS90CF384MTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP	FLINK3V8BT-65
DS90CF364MTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP	FLINK3V6BT-65

Delay/skew units in ns, I_{CC} in mA.

Designing with LVDS

Chapter 4

4.0.0 DESIGNING WITH LVDS

4.1.0 PCB BOARD LAYOUT TIPS

Now that we have explained how LVDS has super speed, and very low power, noise, and cost, many people might assume that switching to LVDS (or any differential technology) will solve all of their noise problems. It will not, but it can help a lot! LVDS has low swing, differential, ≈3.5mA current mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond which means many signal paths act as transmission lines. Therefore, knowledge of ultra-high speed board design and differential signal theory is required. Designing high speed differential boards is not difficult or expensive, so familiarize yourself with these techniques *before* you begin your design.

The speed of LVDS means that impedance matching is very important even for short runs. Matching the differential impedance is as important as matching single-ended impedance. Discontinuities in differential impedance **will** create reflections which will degrade the signal and also show up as common mode noise. Common mode noise on the line will not benefit from the cancelling magnetic field effect of differential lines and will be radiated as EMI. You should use controlled differential impedance traces as soon as you can after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12mm (0.5in). Also, do not make 90° turns since this causes impedance discontinuities, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs which looks like and radiates as common mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are inexpensive and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should be quick and easy to develop.

4.1.1 PC Board

a) **Use at least 4 PCB board layers** (top to bottom): LVDS signals, ground, power, TTL signals.

b) **Isolate TTL signals from LVDS signals**, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

c) Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

d) Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power Supply: A 10µF 35V tantalum capacitor works well between supply and ground. 4.7µF is common, but choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 to 300MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} Pins: Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1µF, 0.01µF, and 0.001µF) in parallel should be used between each V_{CC} pin and ground. The capacitors must be placed as close as possible to the V_{CC} pins. Wide (>4 bits) and PLL-equipped (e.g. Channel Link & FPD Link) LVDS devices should have three capacitors, while other LVDS devices are usually fine with a 0.1µF (possibly also a 0.01µF) capacitor. The bottom line: use good bypassing practices. EMI can be greatly reduced by keeping power and ground planes quiet.

e) **Power and ground should use wide (low impedance) traces.** Do not use 50Ω design rules on power and ground traces.

f) Keep ground PCB return paths short and wide.

g) Cables should employ a ground return wire connecting the grounds of the two systems. See section 5.3.0

h) **Use multiple (at least two) vias to connect to power and ground, traces and planes**. Surface mount capacitors can be soldered directly to these via pads to reduce stubs, though solderability may be impacted.

4.1.2 Traces

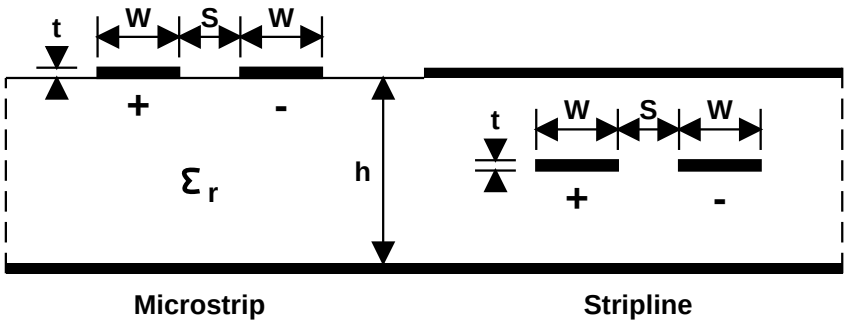
a) Microstrip or stripline both work well.

b) Microstrip offers the advantage that higher differential Z_0 is possible and no extra vias are required.

c) Stripline offers better shielding between signals.

4.1.3 Differential Traces

a) **Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be <10mm long)**. This will help eliminate reflections and ensure noise is coupled as common mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common mode which is rejected by the receiver.



When calculating differential Z_0 (Z_{DIFF}), adjust trace width "W" to alter Z_{DIFF}. Do not adjust "S" which should be the minimum spacing specified by your PCB vendor. You can use National's Transmission Line RapiDesigner slide rule (lit# 633200-001 metric or #633201-001 English units) and app note AN-905, lit# 100905-001) to calculate Z_0 and Z_{DIFF}, or you can use the equations below:

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.48e^{-0.96\frac{s}{h}}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_{DIFF} \approx 2*Z_0 \left(1 - 0.347e^{-2.9\frac{s}{h}}\right) \text{ Ohms} \quad \text{Stripline}$$

where

$$Z_0 \approx \frac{60}{\sqrt{0.475\,E_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_0 \approx \frac{60}{\sqrt{E_r}} \ln\left(\frac{4h}{0.67\,\pi\,(0.8w + t)}\right) \text{ Ohms} \quad \text{Stripline}$$

Use consistent (e.g. centimeters only) dimensions for s, h, w, and t.
Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary.

Common values of dielectric constant (E_r) for various printed circuit board (PCB) materials is given below. Consult your PCB manufacturer for actual numbers. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. Teflon is about four times as expensive as FR-4, but can be considered for 100+MHz designs. Also note that E_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

PCB Material	Dielectric Constant (E_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1-2.5	0.0002-0.002
BT Resin	2.9-3.9	0.003-0.012
Polyimide	2.8-3.5	0.004-0.02
Silica (Quartz)	3.8-4.2	0.0006-0.005
Polyimide/Glass	3.8-4.5	0.003-0.01
Epoxy/Glass (FR-4)	4.1-5.3	0.002-0.02

b) Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/E_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps).

c) Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match
differential impedance and provide isolation for the differential lines.

d) Minimize the number of vias and other discontinuities on the line.

e) **Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.**

f) Within a pair of traces, the distance between the two traces should be minimized to maintain common mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

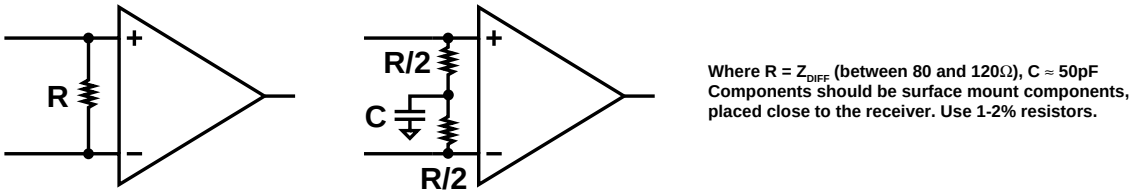
4.1.4 Termination

a) **Use a termination resistor which best matches the differential impedance of your transmission line.** It should be between 90Ω and 130Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS will not work without resistor termination.

b) Typically a single resistor across the pair at the receiver end suffices.

c) Surface mount 1-2% resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7mm (12mm MAX).

d) Center tap capacitance termination may also be used in conjunction with two ≈50Ω resistors to filter common mode noise at the expense of extra components if desired.



Where R = Z_{DIFF} (between 80 and 120Ω), C ≈ 50pF Components should be surface mount components, placed close to the receiver. Use 1-2% resistors.

Common termination schemes.

4.1.5 Unused Pins

a) **Leave unused LVDS receiver inputs open (floating).** Their internal fail-safe feature will lock the outputs high. These unused receiver inputs should not be connected to noise sources like cables or long PCB traces — float them near the pin.

b) Leave all unused LVDS and TTL outputs open (floating) to conserve power.

c) Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground.

4.1.6 Probing LVDS Transmission Lines

a) **Always use a high impedance (>100kΩ), low capacitance (<0.5pF) scope probes with a wide bandwidth (>3GHz) scope.** Improper probing *will* give deceiving results.

4.1.7 Loading LVDS I/O

a) Avoid placing any devices which heavily load the low, ≈3.5mA LVDS output drive. If additional ESD protection devices are desired, use components which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

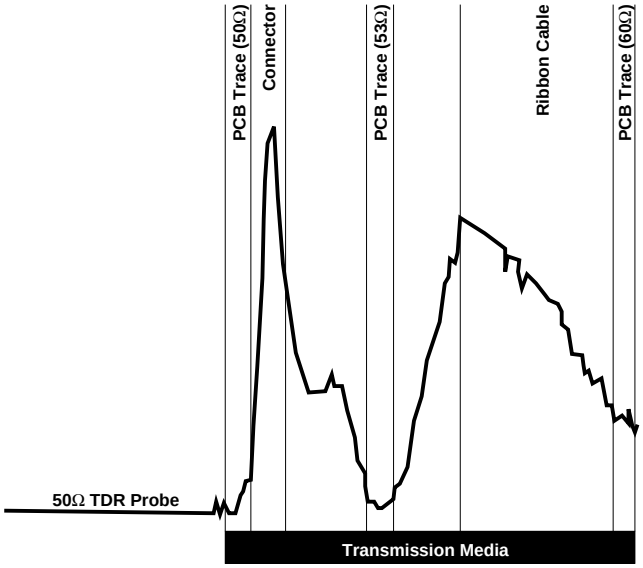
b) Try not to disturb the differential balance. Treat both members of a pair equally.

4.2.0 RESULTS OF GOOD VS. BAD DESIGN PRACTICES

4.2.1 Impedance Mismatches

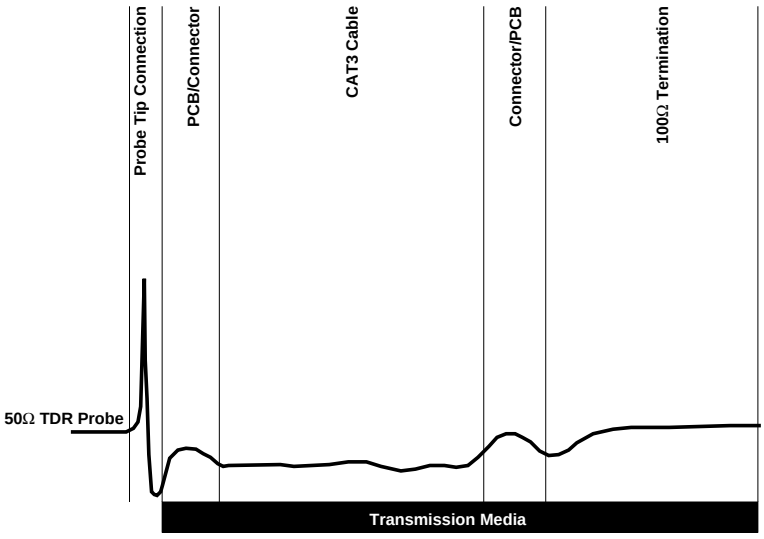
It is very common for designers to automatically use any off-the-shelf cables and connectors and 50Ω autorouting when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable

are not meant for high speed signals (especially differential signals) and do not have controlled impedance. The figure below shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedance are neither matched nor controlled. Beware, this example is not worst case — it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.



TDR plot of transmission media with mismatched impedance.

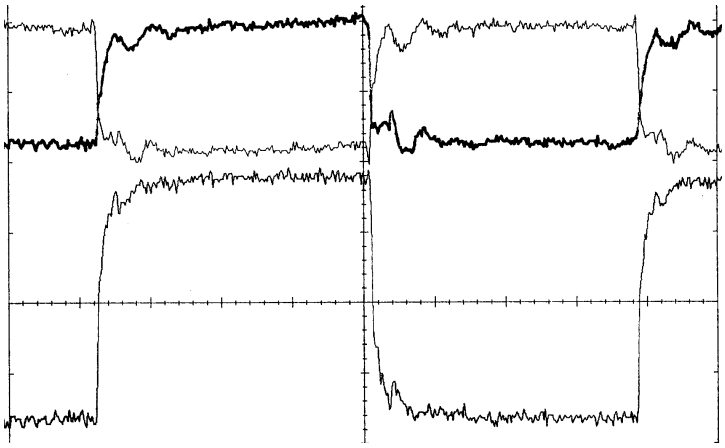
Below is a much improved design which follows most of the high speed differential design practices listed in Section 4.1. The TDR differential impedance plot is much flatter and noise is **dramatically** reduced.



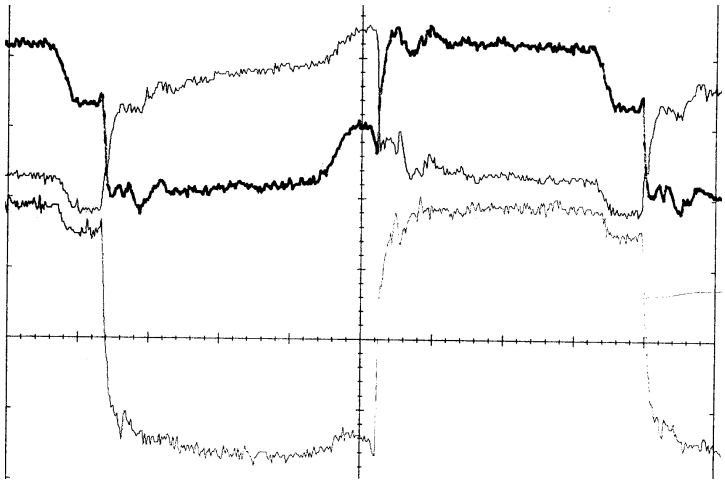
Minimize impedance variations for best performance.

4.2.2 Crosstalk Between TTL and LVDS Signals

The next two figures show the effects of TTL coupling onto LVDS lines. The first figure shows the LVDS waveforms before coupling, while the second shows the effects of a 25MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 inches. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally — the signal which runs closest to the TTL trace is affected more than the other. This difference will not be rejected by the receiver as common mode noise and though it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal reducing noise margin. The common mode noise will be rejected by the receiver, but can radiate as EMI.



LVDS signals before crosstalk.



LVDS signals affected by TTL crosstalk.

In summary, place TTL signals at least 12mm away from LVDS signals or place a power or ground plane between them.

4.3.0 LOWERING ELECTROMAGNETIC INTERFERENCE (EMI)

4.3.1 LVDS and Lower EMI

High speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1) The low output voltage swing (≈350mV)

2) Relatively slow edge rates, dV/dt ≈ 0.350V/0.5ns = 0.7 V/ns

3) Differential (odd mode operation) so magnetic fields tend to cancel

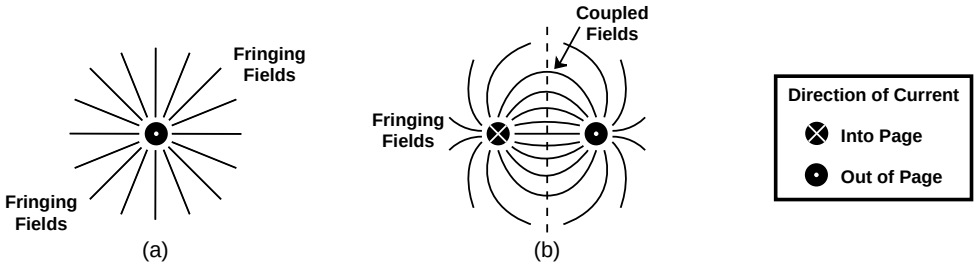
4) "Soft" output corner transitions

5) Minimum I_{CC} spikes due to low current mode operation

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

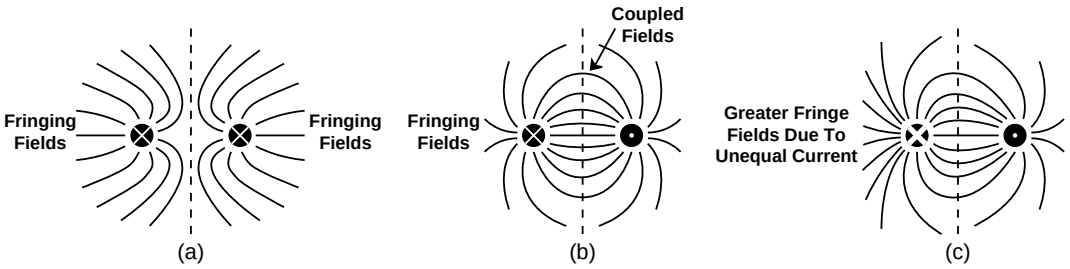
4.3.2 Electromagnetic Radiation of Differential Signals

Today's increasing data rates and tougher electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves which can escape through shielding causing a system to fail EMC tests. Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another). In single-ended lines like CMOS/TTL shown below, almost all the electric field lines are free to radiate away from the conductor. These fields may be intercepted by other objects, but some can travel as TEM waves which may escape the system causing EMC problems.



Electromagnetic field cancellation in differential signals (b) through coupling versus a single-ended signal (a).

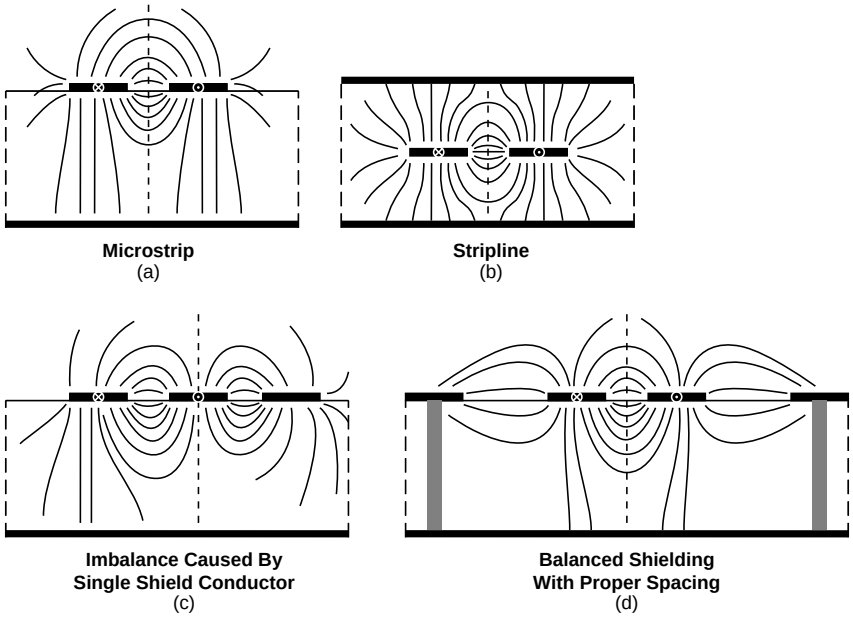
Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic fields lines tend to cancel and the electric fields (shown above) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals much less field energy is available to propagate as TEM waves versus single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.



Even or common mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in (a) above, but factors can cause an imbalance in currents (c) versus the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown below. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_{0DIFF}. More shielding can be achieved using microstrip without significantly impacting propagation velocity using shield traces as in (d), but be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace — or any trace — on one side (c) creates an imbalance which can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2s from the pair.

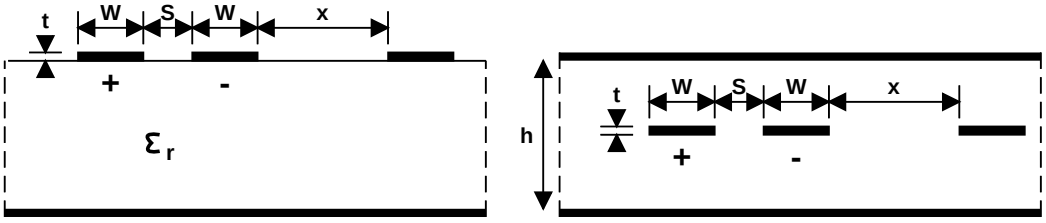


Ideal differential signals on microstrip a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d).

4.3.3 Design Practices for Low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are close coupling between the conductors of each pair and minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown below. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors to preserve closer coupling between the conductors versus the power and ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

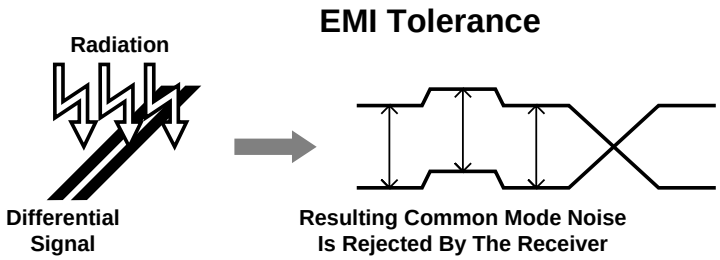


Microstrip **Stripline**

For good coupling, make S < 2W, S < h, and x ≥ 2W & 2S.

For sufficient coupling (cancelling) of electromagnetic fields, "+" and "–" signal distance must be minimized.

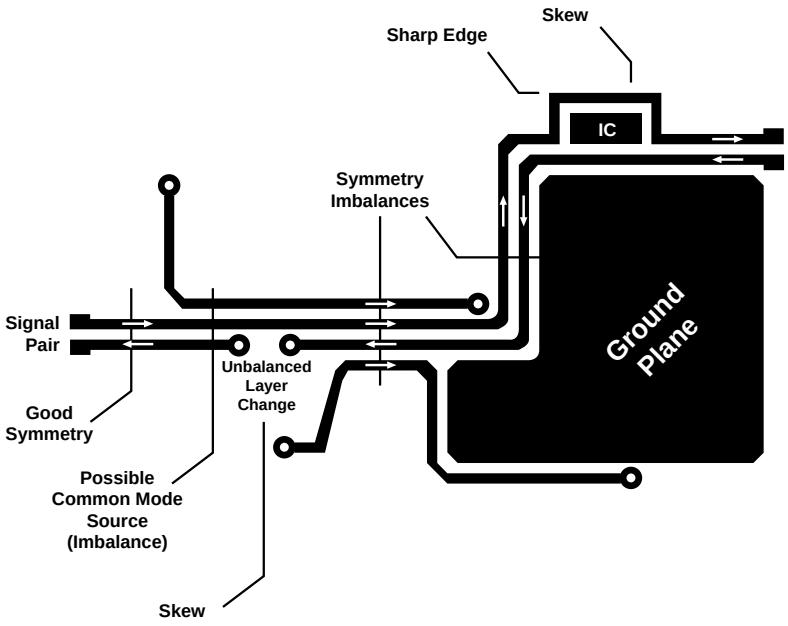
Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common mode noise which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.



Close coupling not only reduces EMI, but improves EMI tolerance too.

Imbalance minimization is the other important factor in reducing EMI. Although fields result from the complex interaction between objects of a system and are difficult to predict (especially in the dynamic case), certain generalizations can be made. The impedance of your signal traces should be well-controlled. If the impedance of one trace changes versus another, the voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should introduced equally to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, PCB traces, etc. Remember, the key word is **balance**.



This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation.

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Since fields are proportional to voltage/current amplitude at any given point in time, any factors affecting the time (delay, velocity, etc.) and/or amplitude (attenuation, etc.) properties of the signals can increase EMI and can be seen on a scope. The next figure illustrates how waveforms — easily seen on a scope — can help predict far field EMI. First, the beneficial field cancelling effects of ideal differential signals (b) versus single-ended signals (a) are compared.

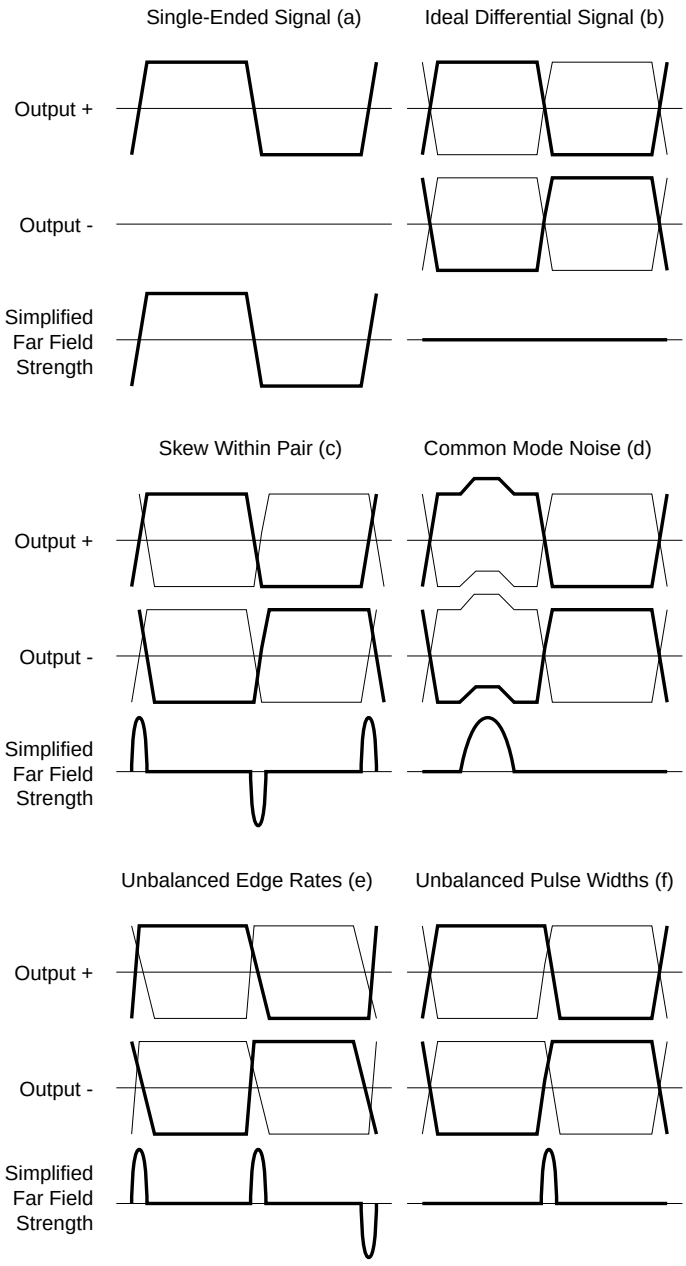
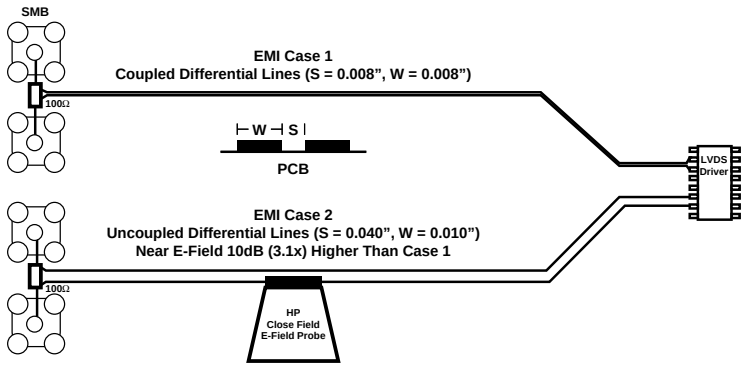


Diagram showing simplified far field radiation under various situations.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common mode noise, unbalanced attenuation, etc. These affect the relative amplitudes of the fields at any given moment, reducing the cancelling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

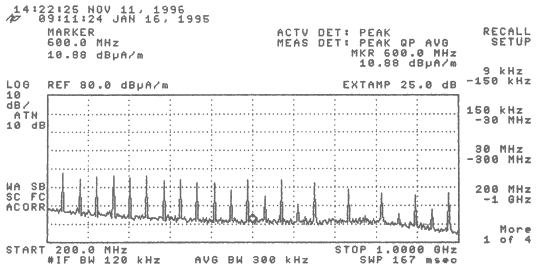
4.3.4 EMI Test Results

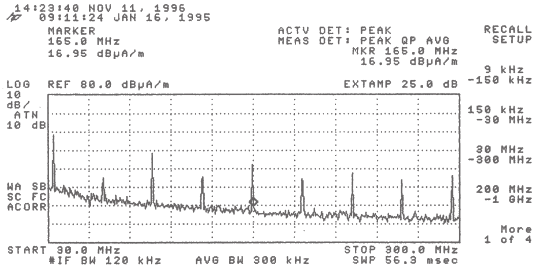
The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals versus uncoupled signals. The setup compares two sets of LVDS signals: one set in which pair spacing is less than trace width (S<W) and another set in which S>>W so that the pair members are no longer closely coupled (though the differential impedance of the transmission line is still 100Ω).



EMI Test Setup

Near (close) field electric field measurements were made for both cases while using a 32.5MHz 50% duty cycle clock as the source. The two plots below show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200MHz to 1GHz. The second plot looks more closely at the frequencies between 30MHz and 300MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.

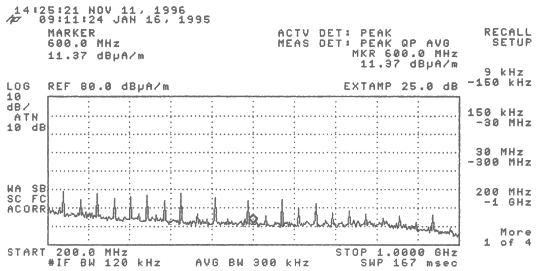


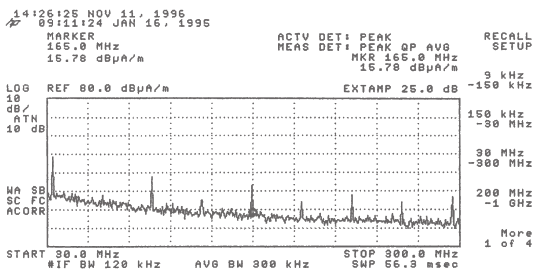


Near E-Field Strength for Uncoupled Signals

(Case 2): 200MHz-1GHz *(Case 2): 30MHz-300MHz*

The next two plots show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.





Near E-Field Strength for Closely Coupled Signals

(Case 1): 200MHz-1GHz *(Case 1): 30MHz-300MHz*

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The closely coupled pair showed about 10dB (>3 times) lower electric field strength than the uncoupled pair.

This test illustrates two things:

1) Use of differential signals versus single-ended signals can be used effectively to reduce emissions.

2) The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than is seen here.

4.3.5 Ground Return Paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least impedance.

Since LVDS is differential, differential current that flows in one conductor of a pair will flow back through the other conductor, completing the current loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common mode noise current which must return also. This common mode current will be capacitively coupled to ground and return to the driver through the path of least impedance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems as well as single-ended (though to a lesser extent).

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least impedance and means that the current loop area is minimized.

Similarly, in cable ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area (see Chapter 5).

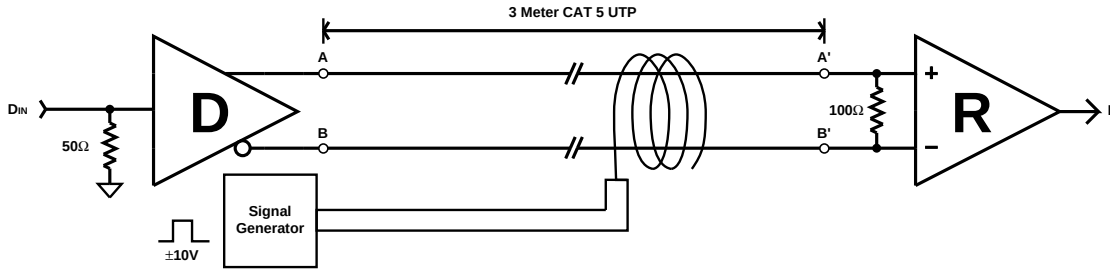
4.3.6 Cable Shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Many shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (see Chapter 5).

4.3.7 Conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled.

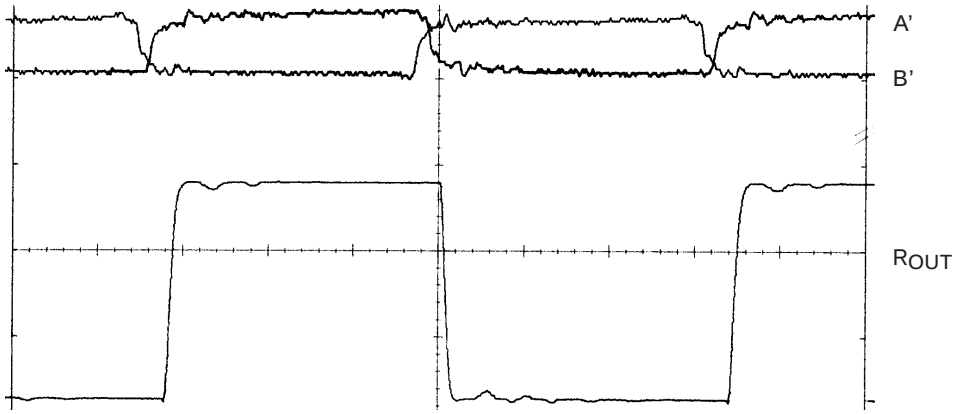
4.4.0 COMMON MODE NOISE REJECTION



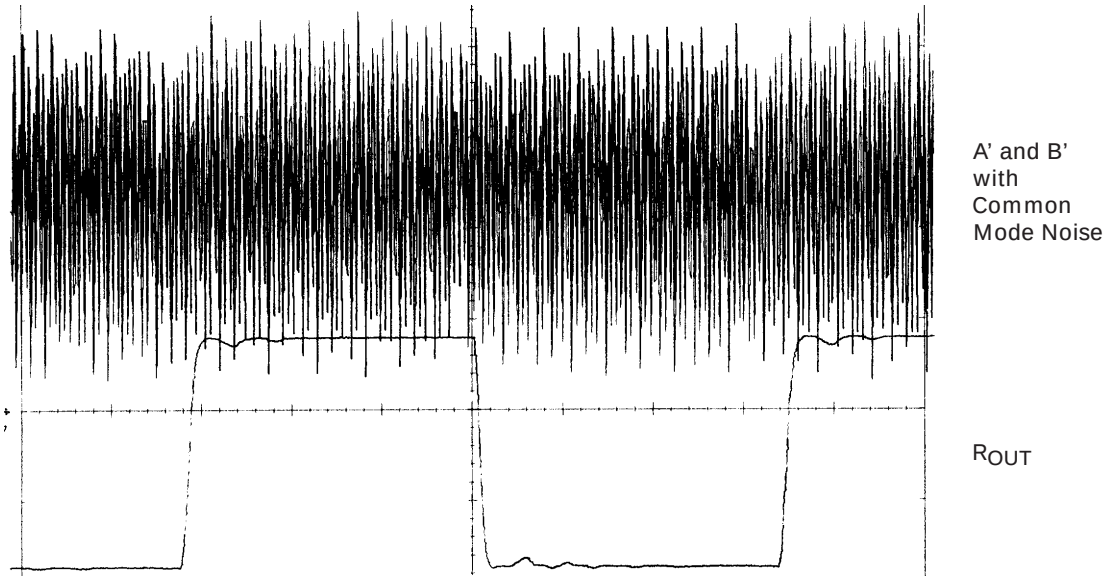
Common mode noise rejection test setup.

Test Setup:
Driver: DS90C031 (one channel)
Receiver: DS90C032 (one channel)
V_{CC} = 5V
T = 25°C

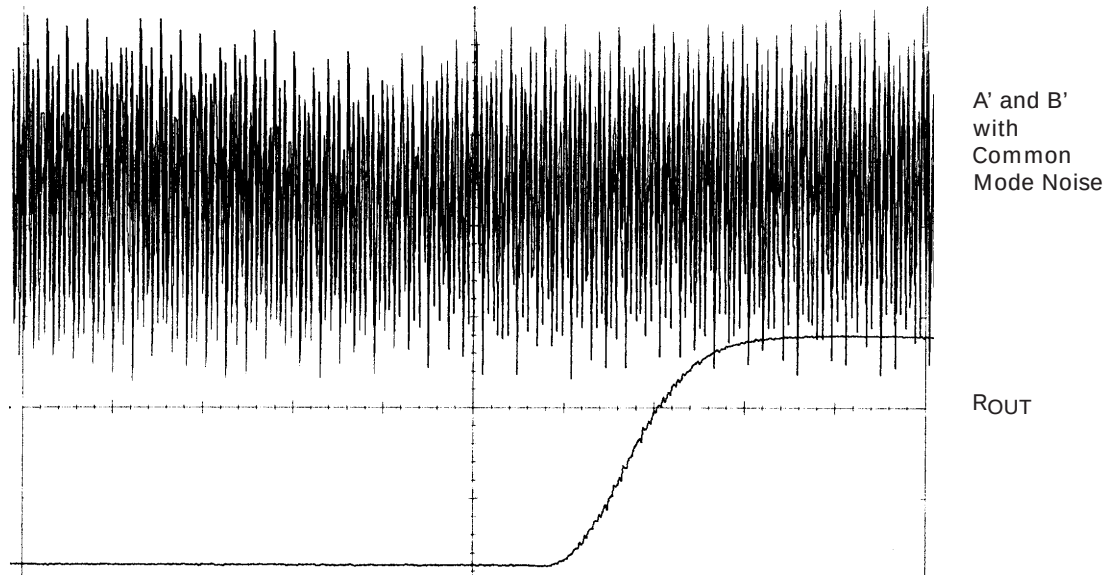
This test demonstrates the common mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (≈±350mV swing with <±100mV thresholds). Provided that the differential signals run close together through controlled impedance media, however, most of the noise on LVDS lines will be common mode. In other words, EMI, crosstalk, power/ground shifts, etc. will appear equally on each pair and this common mode noise will be rejected by the receiver. The plots below show common mode noise rejection with VCM noise up to –0.5V to +3.25V peak-to-peak.



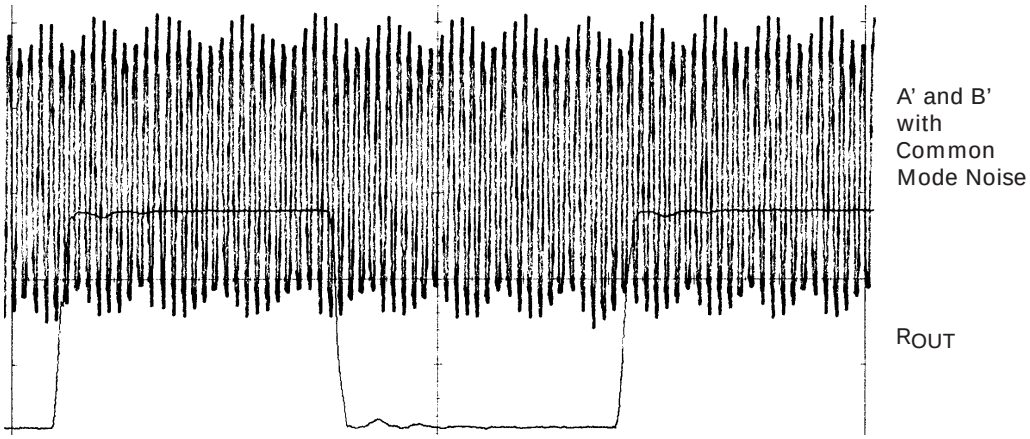
Reference waveform showing LVDS signal and receiver output.



Coupled common mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.

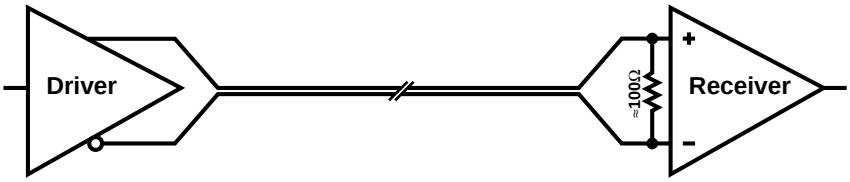


Expanded view of coupled common mode noise waveform and clean receiver output.



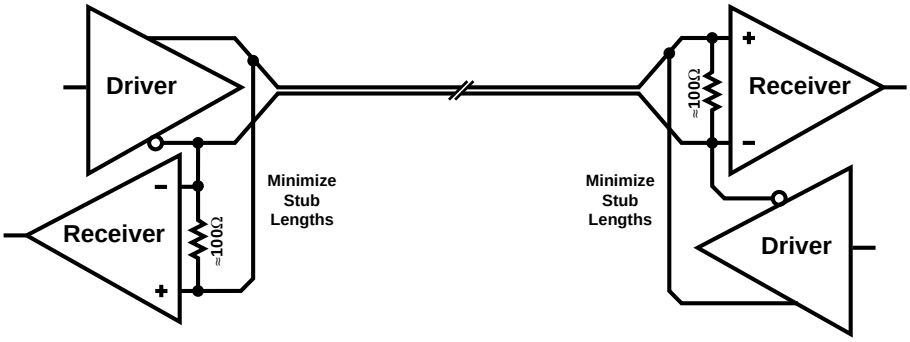
Clean receiver output despite –0.5V to +3.25V peak-to-peak common mode noise.

4.5.0 LVDS CONFIGURATIONS

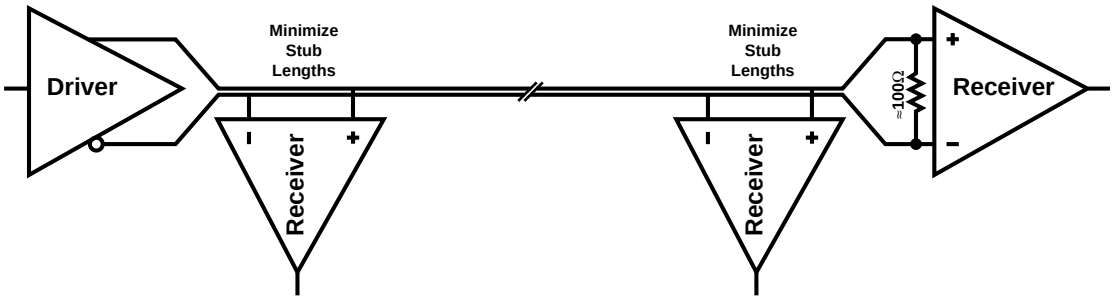


Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The configuration shown below allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (≤10m). Typical LVDS I/O capacitances are 5-7 pF for receiver inputs and 3.5-4pF for driver outputs.



Bi-directional half-duplex configuration.



Multidrop configuration.

Since LVDS receivers have high impedance inputs, a multidrop configuration can also be used if transmission distance is short and stub lengths are less than 12mm (<7mm is recommended). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down.

4.6.0 FAIL-SAFE FEATURE

4.6.1 Most Applications

To help ensure reliability, LVDS receivers have internal fail-safe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Here is a summary of LVDS fail-safe conditions:

1) Open Input Pins
   Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state.

2a) Terminated Input Pins
   If the driver is in a TRI-STATE® condition, in a power-off condition, or is disconnected (cable unplugged), the receiver output will be in a high state, even with the termination resistor across the input pins.

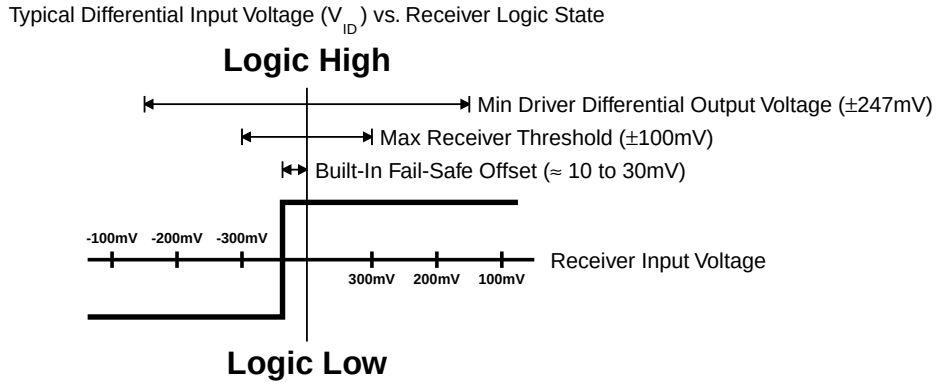
2b) Terminated Input Pins — Noisy Environments
   See section 4.6.2 if fail-safe must be guaranteed in noisy environments when the cable is disconnected from the driver end or the driver is in TRI-STATE®.

3) Shorted Inputs
   The receiver output will remain in a high state when the inputs are shorted.

4.6.2 Boosting Fail-Safe In Noisy Environments

The internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection for floating receiver inputs, shorted receiver inputs, and terminated receiver inputs. It is not designed to provide fail-safe in noisy environments when the cable is disconnected from the driver end or the driver is TRI-STATE. When this happens, the cable becomes a floating antenna which can pick up noise. If the cable picks up more differential noise than the internal fail-safe circuitry can overcome, the receiver may switch or oscillate. If this condition can happen in your application, it is recommended that you choose a balanced and/or shielded cable which will reduce the amount of differential noise on the cable. In addition, you may wish to add external fail-safe resistors to create a larger noise margin. However, adding more fail-safe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore a compromise should be the ultimate goal.

4.6.3 Choosing External Fail-Safe Resistors



External fail-safe can be added, but must be small enough not to significantly affect driver current.

The chart above shows that National's present LVDS devices typically have an internal fail-safe voltage of about 10 to 30mV. If the receiver will not always be driven by the driver in your application and the cable is expected to pick up more than 10mV of differential (not common mode) noise you may need to add additional fail-safe resistors. The resistors are chosen by first measuring the amount of differential mode noise you will need to overcome, V_{FSB}, by biasing the termination resistor (≈100Ω) to generate this voltage. Note that you do not need to provide a bias, V_{FSB}, which is greater than the receiver threshold (100mV). You only need enough to overcome the differential noise, since the internal fail-safe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

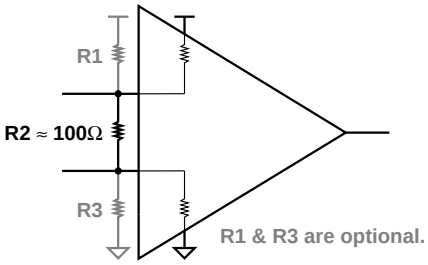


Diagram showing simplified internal fail-safe circuitry and optional external "helper" fail-safe resistors.

For best results, follow these procedures when choosing external fail-safe resistors:

1) First ask the question "Do I need external fail-safe?" If your LVDS driver is always active, you will not need external fail-safe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential mode noise you may not need to boost fail-safe.

2) Measure the amount of **differential (odd) mode** noise at the receiver end of the cable in worst case conditions. If you have a lot of noise, **use a balanced cable** like twisted pair which tends to pick up mostly common mode noise , not differential mode noise. Do not use simple ribbon or coax cables which can pick up differential mode noise.

   Use a **shielded cable** if possible. Using a balanced and/or shielded cable is best way to prevent instead of fix the noise issue!

3) Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst case conditions. Set this equal to V_{FSB} in the equation below and solve for the external fail-safe resistors R1 and R3.

$$V_{FSB} = \frac{R2}{R1 + R2 + R3} V_{CC}$$

$$I_{BIAS} = \frac{V_{CC}}{R1 + R2 + R3} << I_{LOOP} \quad (\text{Use } I_{BIAS} \leq 0.1 * I_{LOOP})$$

$$V_{CM} = \frac{R3 + R2/2}{R1 + R2 + R3} V_{CC} = 1.2V \Rightarrow R1 \approx R3 \left(\frac{V_{CC}}{1.2V} - 1 \right)$$

$$R_{TEQ} = \frac{R2\,(R1 + R3)}{R1 + R2 + R3} = \text{match transmission line } Z_{0DIFF}$$

4) You now have an equation relating R1 to R3. Choose R1 and R2 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R2 should be greater than 20kΩ for V_{CC} = 5V and greater than 12kΩ for V_{CC} = 3.3V. **Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.**

5) The external fail-safe resistors may change your equivalent termination resistance, R_{TEQ}. Fine tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

4.7.0 POWER OFF HIGH IMPEDANCE

Power off high impedance is a useful feature:

1) For receivers which might be powered down while the driver is active. Note that since LVDS drivers only source about 3.5mA of current, NOT having power off high impedance may be acceptable.

2) For receivers in multi-drop mode when the network must remain operational if one or more receivers are powered down.

3) For drivers, receivers, and transceivers in multi-point or bidirectional applications when the network must remain operational if one or more receivers are powered down or live insertion capability is desired.

LVDS devices will behave differently during power down. Here is a summary of power off conditions and the results to various devices:

a) Driver power OFF, receiver power ON:

- LVDS receivers have fail-safe to avoid oscillation.
- LVDS quad, dual, and single receivers outputs will be locked to logic high.
- LVDS Channel Link and FPD-Link device outputs will remain in last known state until clocked at which point the outputs will lock high.
- Some driver outputs will power off to high impedance (check datasheet).

b) Driver power ON, receiver power OFF:

- 5V receivers will sink driver current, but since this current is small, it will not damage the driver (transmitter) or receiver.
- 3V receiver inputs will power off to high impedance.

Cables and Connectors

Chapter 5

5.0.0 MEDIA (CABLE AND CONNECTOR) SELECTION

5.0.1 General Comments

When choosing cables and connectors for LVDS it is important to remember:

1) Use controlled impedance media. The cables and connectors you use should have a matched differential impedance of about 100Ω. They should not introduce major impedance discontinuities.

2) Balanced cables (e.g. twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common mode (not differential mode) noise which is rejected by the receiver.

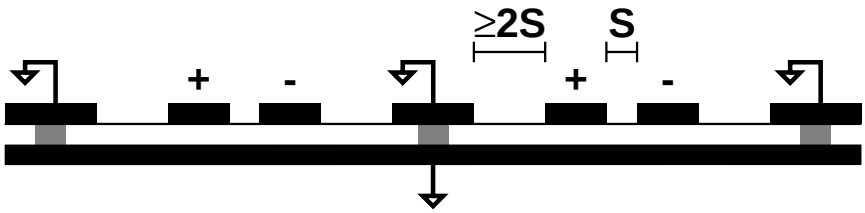
3) For cable distances <0.5m, most cables can be made to work effectively. For distances 0.5m ≤ d ≤ 10m, CAT 3 (category 3) twisted pair cable works well and is readily available and relatively inexpensive. For distances >10m, and high data rates CAT 5 twisted pair is recommended.

5.2.0 CABLING SUGGESTIONS

As described above, try to use balanced cables (twisted pair, twinax, or flex circuit with closely coupled differential traces). Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

5.2.1 Flex Circuit

Flex circuit is a good choice for short runs, but it is difficult to shield.



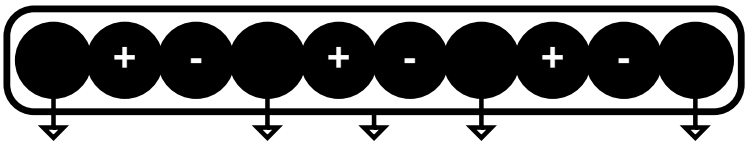
a) Closely couple the members of differential pairs (S<W). Do not run signal pairs near the edges of the cable.

b) Use a ground plane.

c) Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

5.2.2 Ribbon Cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well-suited for high speed differential signaling (good coupling is difficult to achieve), but it is OK for short runs.

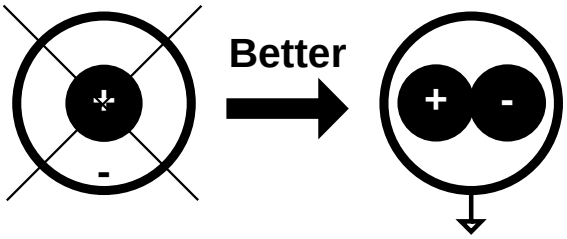


a) If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.

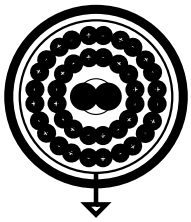
b) Use shielded cable if possible.

5.2.3 Twinax and Coax

Coax is not balanced, so twinax is much better for LVDS.



5.2.4 Twisted Pair

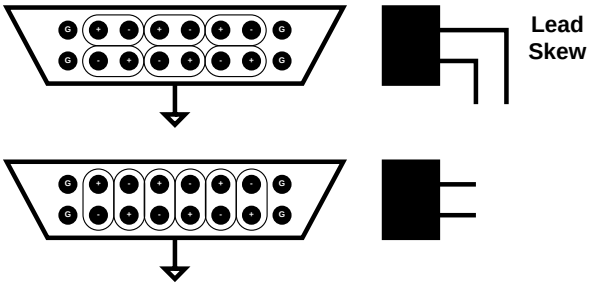


a) Twisted pair is a good choice for LVDS. Category 3 (CAT3) cable is good for runs up to about 10m, while CAT5 is better for longer runs.

b) For lowest skew, group skew-dependent pairs together (towards the center or towards the outside of the cable).

c) Ground and/or terminate unused conductors.

5.2.5 Connectors



a) Choose low skew, impedance matching connectors if possible.

b) Group members of each pair together. **Be sure that the pin assignment you choose on the connector matches the orientation of the pairs. In other words, a pair may be pins 1 and 26 not pins 1 and 2.**

c) Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins which yield the lowest skew and crosstalk for your particular connector.

d) Place ground pins between pairs where possible and convenient.

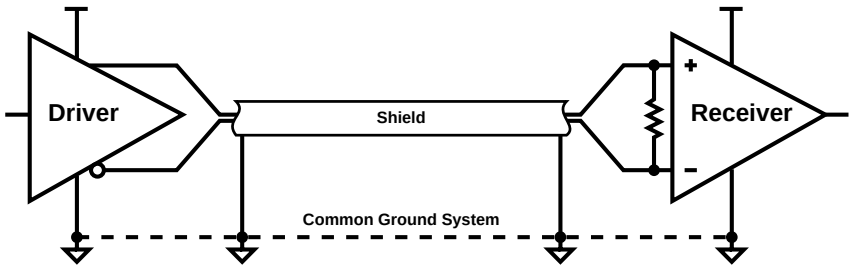
e) Ground end pins. Do not use end pins for high speed signals.

f) Ground and/or terminate unused pins.

5.3.0 CABLE GROUND AND SHIELD CONNECTIONS

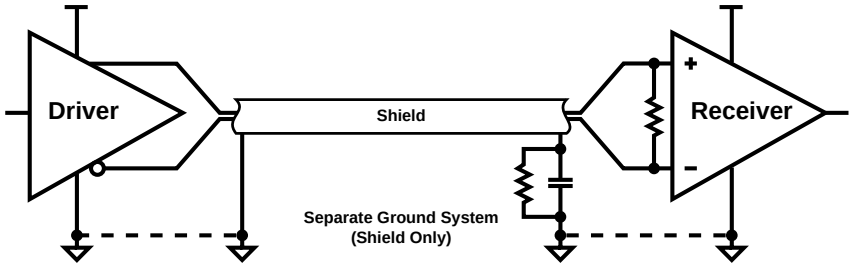
In many systems, cable shielding is required for EMC compliance. Although LVDS provides low EMI benefits when used properly, shielding is still usually a good idea. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the shield in some cables) provides a small loop area AC return path for common mode currents. **Note: it is beyond the scope of this book to effectively deal with cabling systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding and grounding.**

5.3.1 Common Ground Systems

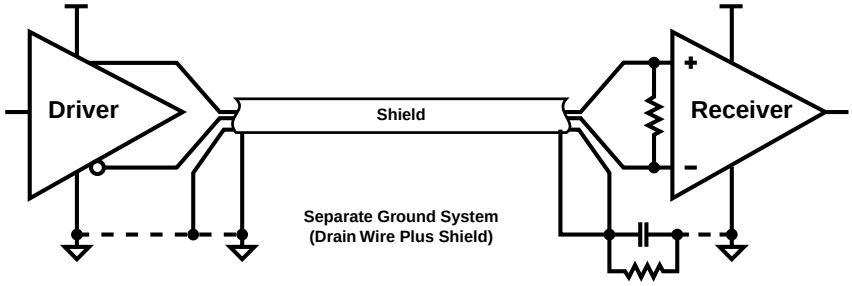


In applications where the grounding system will be common to both the receiver and the driver, the cable shield is connected at both ends (DC connection) to the common ground. Avoid “pig-tail” ground wiring from the cable. In the case where connectors are involved that penetrate the system’s enclosure, the cable shield must have a circumferential contact to the connector’s conductive backshell.

5.3.2 Separate Ground Systems



Where AC and/or DC voltage potentials exist between the driver and receiver sub-systems or where these do not share a common ground system, the cable shield should be connected to the receiver's ground system via a capacitor of suitable value and voltage rating to handle the average DC and peak AC voltages that may be present. A "bleeder resistor" should be connected across the capacitor. The value of this resistor (and capacitor) may be governed by safety requirements (UL, CSA, VDE, BS, or other) or other statutory requirements. Care should be taken when selecting the resistor value so as not to allow potentially lethal voltages to be developed across it.



When the cable has an integral drain wire and a woven braid shield, both are connected together at the driver and receiver ends and treated as a common shield conductor. For non-metallic shield materials (like aluminized mylar) with a drain wire, treat the drain wire a s the shield connection as in the cases described for metallic shields.

5.4.0 LVDS SIGNAL QUALITY: JITTER MEASUREMENTS USING EYE PATTERNS

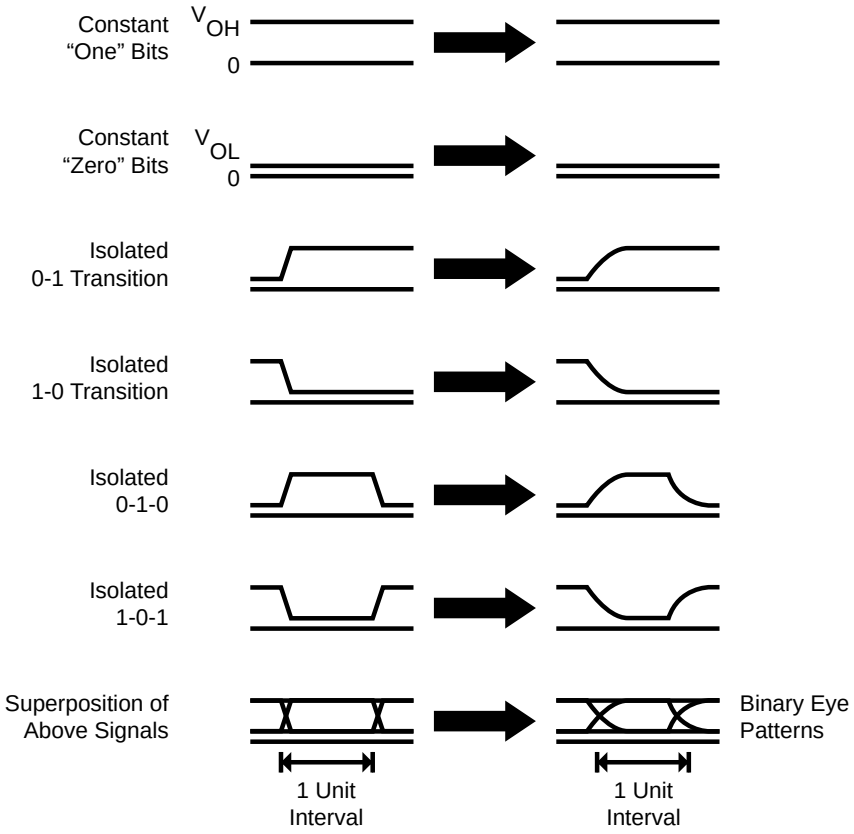
5.4.1 LVDS Signal Quality

This report provides data rate versus cable length recommendations for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and printed circuit board (PCB). Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment — or even better — in the actual application. Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

5.4.2 Why Eye Patterns?

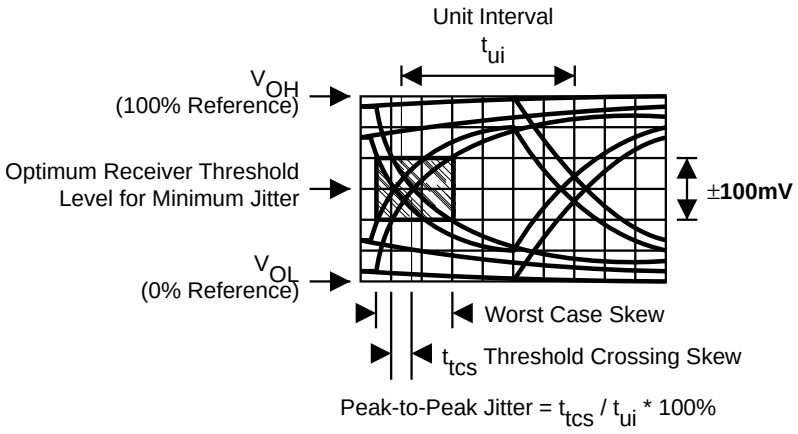
The eye pattern is used to measure the effects of inter symbol interference on random data being transmitted through a particular medium. The transition time of the signal is effected by the prior data bits. This is especially true for NRZ data which does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects that the cable causes. The figure below illustrates the superposition of six different data patterns. Overlaid they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider, and the opening of the eye is also now smaller (see application note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter symbol distortion as is a data line.



Formation of an Eye Pattern by Superposition.

The figure below describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between –100mV and +100mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100mV and jitter measured between the first and last crossing at ±100mV. If the vertical axis units in the figure were 100mV/division, the worse case jitter is at ±100mV levels.



NRZ Data Eye Pattern.

5.4.3 Eye Pattern Test Circuit

LVDS drivers and receivers are intended to be primary used in an uncomplicated point-to-point configuration as shown in the figure below. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) l28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer that 10 meters were not tested, but may be employed at lower data rates.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

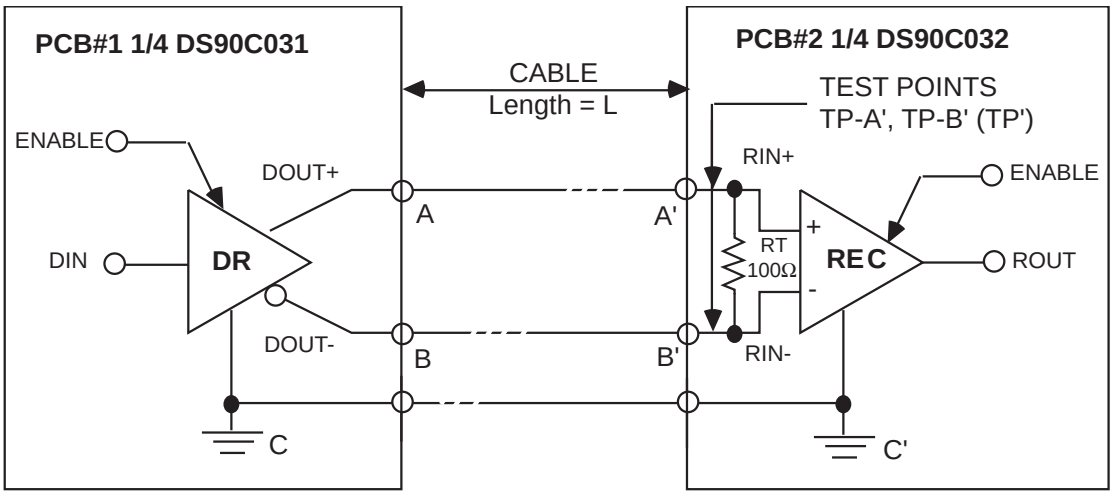


Figure 3. LVDS Signal Quality Test Circuit

5.4.4 Test Procedure

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. First, jitter was measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone, this will result in a much lower jitter point, but ignores the fact that the receivers may not switch at that very point. For this reason this signal quality test report measured jitter at both points.

5.4.5 Results and Data Points

20% Jitter Table @ 0V Differential (Minimum Jitter)

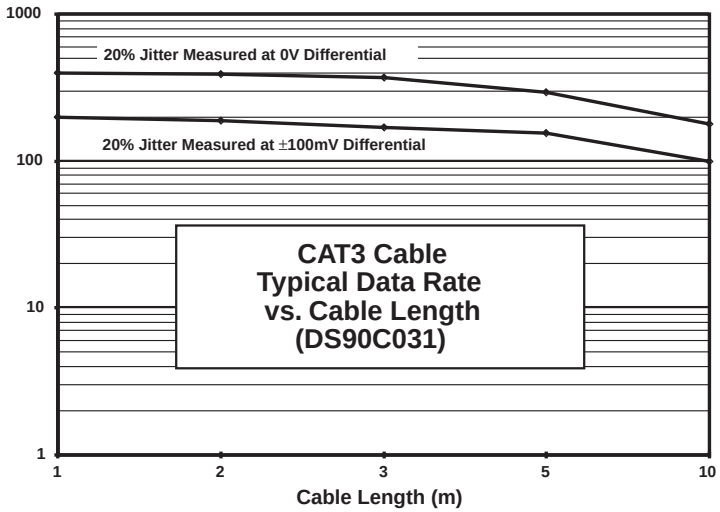
Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the 0V differential point. For the case with the 1 meter cable, 490ps of jitter at 400Mbps was measured, and 1.160ns of jitter at 180Mbps and with the 10 meter cable.

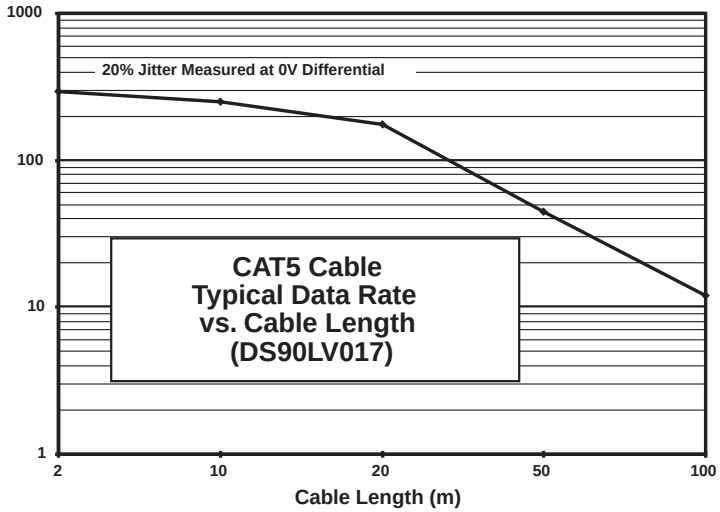
20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100mV levels. For the 1 meter cable, 1ns of jitter was measured at 200Mbps, and for the 10 meter cable, 2ns of jitter occurred at 100Mbps.



Typical Data Rate vs. Cable Length for 0-10m CAT3 Cable.



Typical Data Rate taken just prior to printing this document for 2-100m CAT5 Cable

The figures above are a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200-400 Mbps are possible on the shorter lengths, and rates of 100-200Mbps are possible at 10 meters. Note that employing a different coding scheme, cable, wire gauge (AWG), etc. will create a different relationship between maximum data rate versus cable length. Designers are greatly encouraged to experiment on their own.

5.4.6 Conclusions

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate versus distance for a common, inexpensive type of cable.

5.5.0 BIT ERROR RATE (BER) TESTING

5.5.1 LVDS Cable Driving Performance

The questions of: “How Far?” and “How Fast?” seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example — see application note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector, and information about the printed circuit board (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/2 LVDS Quad Line Driver/Receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

5.5.2 What is a BER Test?

Bit Error Rate testing is one way to measure of the performance of a communications system. The standard equation for an bit error rate measurement is:

Bit Error Rate = (Number of Bit errors) / (Total Number of Bits)

Common measurement points are bit error rates of:

$<1 \times 10^{-12}$ => One or less errors in 1 trillion bits sent

$<1 \times 10^{-14}$ => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance bench mark. For example if the data rate is 50Mbps, and the bench mark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

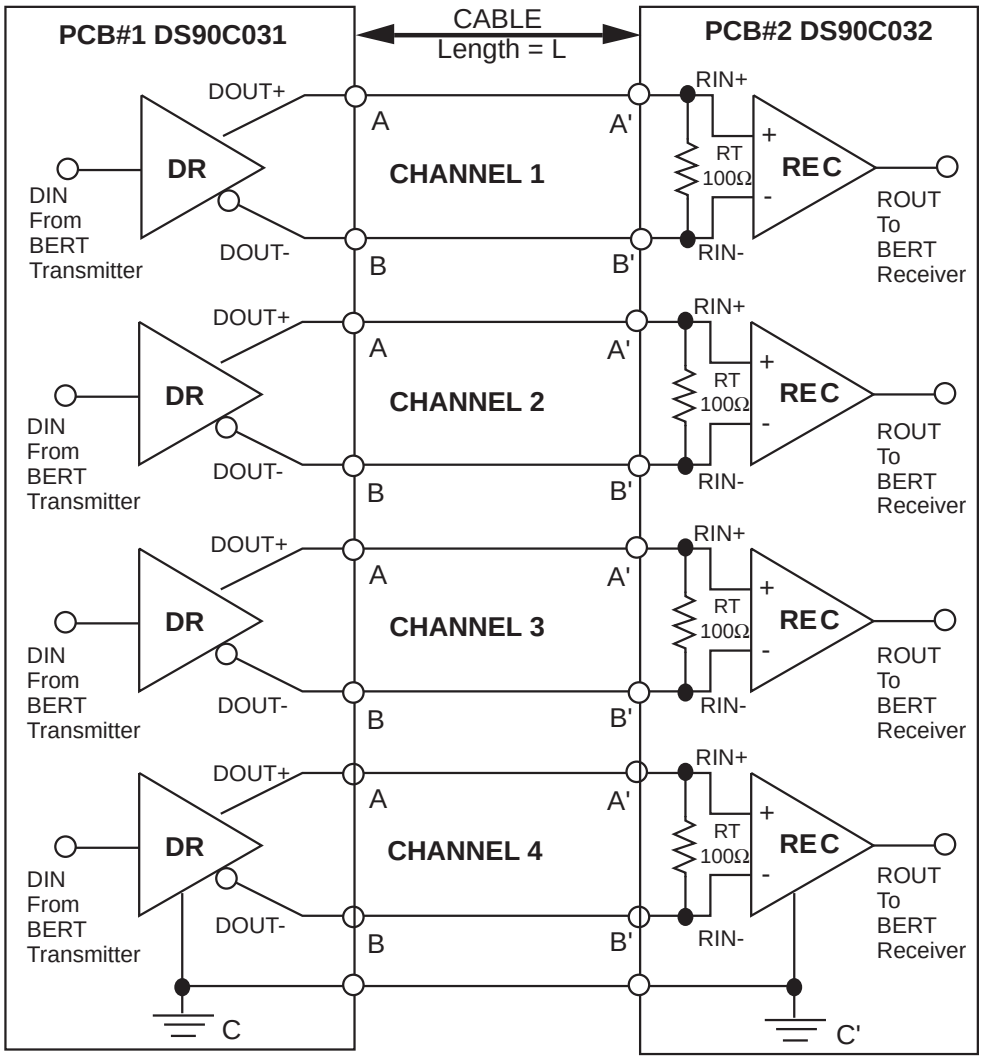
5.5.3 BER Test Circuit

LVDS drivers and receivers are intended to be primary used in an uncomplicated point-to-point configuration as shown in Figure 1. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) 28 AWG stranded twisted pair cable (25 Pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS BER test circuit.

5.5.4 Test Procedure

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of 2^{15}-1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4 bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block the results were recorded which included: elapsed seconds, total bits transmitted, and number of bit errors recorded. For the three tests documented below, a power supply voltage of +5.0V was used, and the tests were conducted at room temperature.

5.5.5 Tests and Results

The goal of the tests was to demonstrate errors rates of less than <1 x 10-12 are obtainable.

TEST #1 Conditions:
- Data Rate = 50Mbps
- Cable Length = 1 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

TEST #1 Results:
- Total Seconds: 87,085 (1 day)
- Total Bits: 1,723 x 1013
- Errors = 0
- Error Rate = < 1 x 10^{-12}

TEST #2 Conditions:
- Data Rate = 100Mbps
- Cable Length = 1 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:
- Total Seconds: 10,717 (~3 hr.)
- Total Bits: 4.38 x 1012
- Errors = 0
- Error Rate = < 1 x 10^{-12}

TEST #3 Conditions:
- Data Rate = 100Mbps
- Cable Length = 5 meter
- PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:
- Total Seconds: 10,050
- Total Bits: 4 x 1012
- Errors = 0
- Error Rate = < 1 x 10^{-12}

5.5.6 Conclusions

All three of the tests ran error free and demonstrate extremely low bit error rates using LVDS technology. The tests concluded error rates of < 1 x 10^{-12} can be obtained at 100Mbps operation across 5 meters of twisted pair cable. BER tests only provide a "Go — No Go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50Mbps to 100Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

LVDS Evaluation Boards

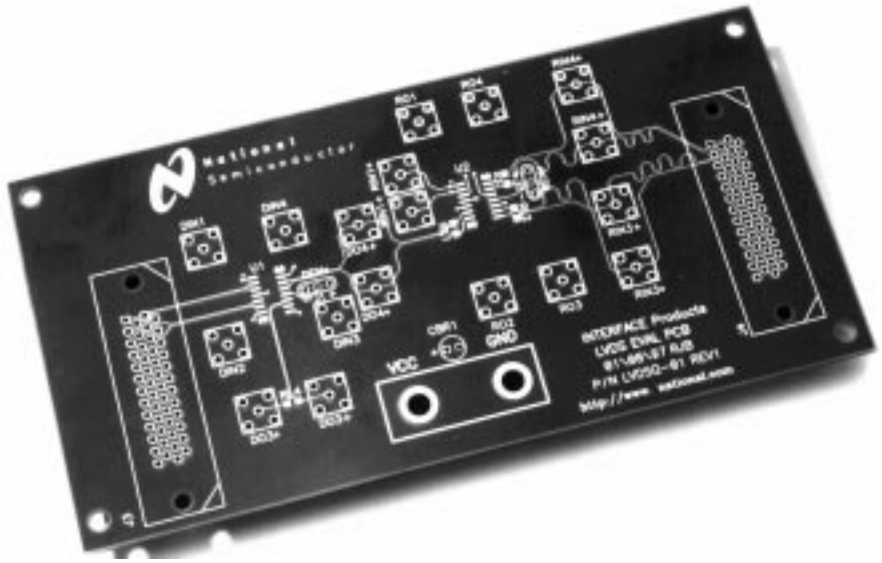
Chapter 6

6.0.0 LVDS EVALUATION BOARDS

Presently there are two types of evaluation boards available: The high speed link (includes Channel Link and FPD-Link) evaluation boards and the Generic LVDS Evaluation Board. (See the selection tables in chapter 3 for a cross reference list of boards versus devices.) The high speed link evaluation boards can be ordered through National's distributors and come complete with a transmitter board, receiver board, ribbon cable, instructions, and datasheets.

FPD-Link Evaluation Board (the Channel Link evaluation board is similar)

These boards are fully populated. TTL signals are accessed through a 50-pin IDC connector on the transmitter and receiver boards. The boards are interconnected via a ribbon cable that can be modified for custom lengths. These evaluation boards are useful for analyzing the operation of National's high speed Channel Link and FPD-Link devices in your system. For LVDS signal quality measurements over other interconnect media, use the Generic LVDS evaluation board.



The Generic LVDS Evaluation Board

The Generic LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over PCB trace, twisted pair cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the LVDS I/O characteristics of most of National's LVDS devices.

a) Use the DS90C031/032 to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.

b) Use the DS90LV031/032 to represent the LVDS I/O characteristics of the DS90LV031/032/017/027 devices.

c) Use the upcoming DS90LV031A/032A (available in October 1997) to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices not listed in (b) above.

The remainder of this chapter is devoted to explaining the operation of the Generic LVDS Evaluation board.

6.1.0 THE GENERIC LVDS EVALUATION BOARD

6.1.1 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of twisted pair cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation PCB is LVDSEVAL-001 (stuffed) or Literature number 550061-001 (unstuffed - limit one per Customer, while supplies last). In this application note and on the PCB the following differential signal nomenclature has been used: "A" represents the true signal and "B" represents the inverting signal. Driver input signals are represented with an "I" while receiver outputs are with an "O."

6.1.2 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately next. Note that the driver / receiver numbers do not directly map to the LVDS test channel number (LVDS Channel 1 utilizes driver number 1 and receiver number 4). The five test cases are shown in figure 1.

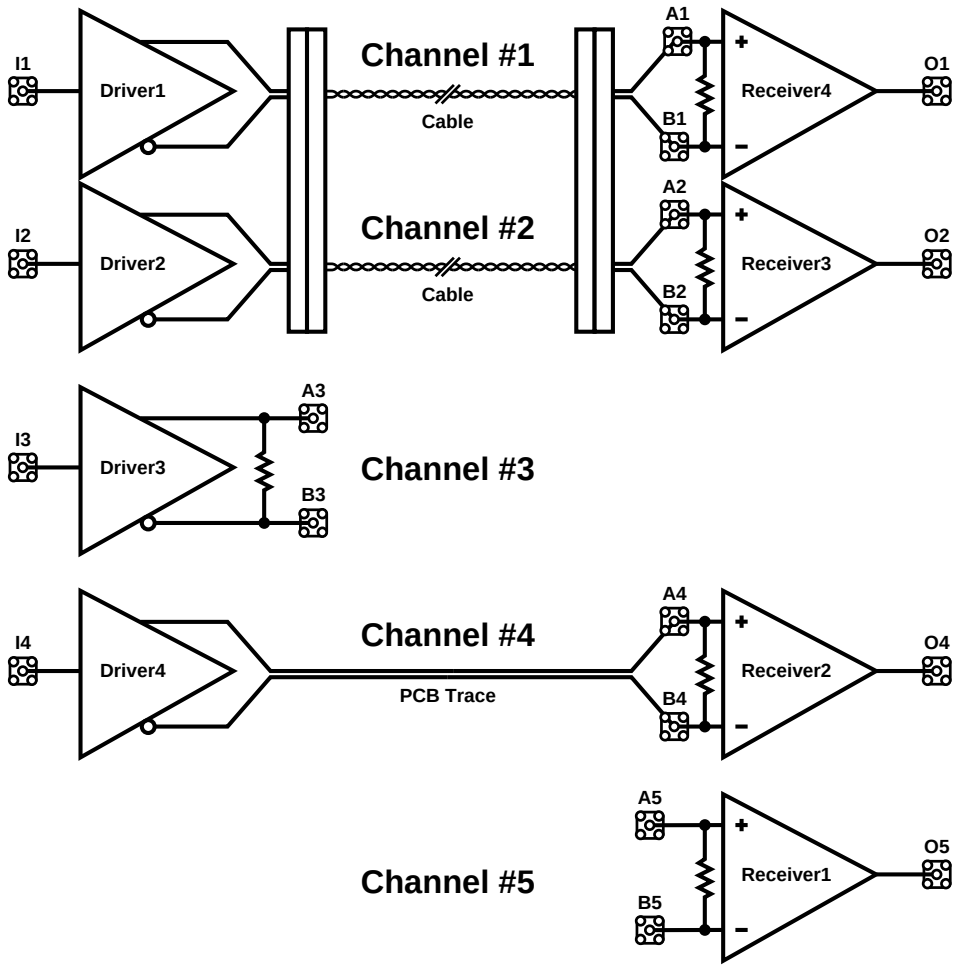


Figure 1: PCB Block Diagram

LVDS Channel # 1: Cable Interconnect

This test channel connects Driver #1 to Receiver #4 via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I1) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A1 and B1. The receiver output signal may be probed at test point O1. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal (see options section). A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A1 and B1.

LVDS Channel # 2: Cable Interconnect

This test channel connects Driver #2 to Receiver #3 also via the cable interconnect. A SMB test point interface is provided at the receiver input side of the cable. The driver input signal (I2) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. LVDS signals are probed via test points A2 and B2. The receiver output signal may be probed at test point O2. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A2 and B2. This channel duplicates channel #1 so that it may be used for a clock function or for cable crosstalk measurements.

LVDS Channel # 3: LVDS Line Driver

This test channel provides test points for an isolated driver with a standard 100 Ohm differential termination load. Probe access for the driver outputs is provided at test points A3 and B3. The driver input signal (I3) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB.

LVDS Channel # 4: PCB Interconnect

This test channel connects Driver #4 to Receiver #2 via a pure PCB interconnect. A SMB test point interface of the LVDS signaling is provided at test points A4 and B4. The driver input signal (I4) is terminated with a 50 Ohm termination resistor on the bottom side of the PCB. The receiver output signal may be probed at test point O4. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. A direct probe connection is possible with a high impedance probe (>100 k Ohm loading) on the LVDS signals at test points A4 and B4. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel # 5: LVDS Receiver

This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either a 100 Ohm resistor connected across the inputs (differential) or two separate 50 Ohm terminations (each line to ground). The second option allows for a standard signal generator interface. Input signals are connected at test points A5 and B5. A PCB option for a series 450 Ohm resistor is also provided in case 50 Ohm probes are employed on the receiver output signal. The receiver output signal may be probed at test point O5.

6.1.3 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a 25 pair (50-pin) SCSI-2 cable commonly referred to as an “A” cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the SCSI-2 standard and the cable is widely available. The connector is 50 position, with 0.050 centers and the pairs are pinned out up and down. For example pair 1 is on pins 1 and 26, not pins 1 and 2.

IMPORTANT NOTE: The 23 unused pairs and the overall shield are connected to ground. Other cables may also be used if they are built up.

6.1.4 PCB Design

Due to the high speed switching rates obtainable by LVDS a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal (TTL/CMOS).

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, see PCB layout between U1 and J3). Employing differential traces will ensure a low emission design and maximum common mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common mode. Also by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable’s differential characteristic impedance). Equations for calculating differential impedance are contained in chapter 4 of the LVDS Owner’s Manual and also in National application note AN-905 for both microstrip and stripline differential PCB traces.

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor minimizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13 mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match the higher the signal fidelity and the less common mode reflections will occur (lower emissions too). Typical values are 100 or 121 Ohm ±5% (media specific).

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

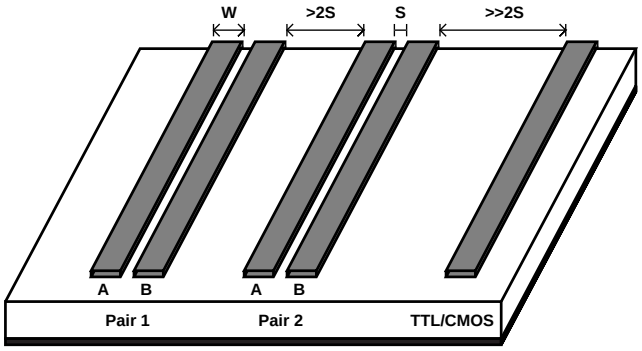


Figure 2: Pair Spacing for differential lines

Bypassing capacitors are recommended for each package. 0.1 µF is sufficient on the quad driver or receiver device (CB2 and CB3) however, additional smaller value capacitors may be added (i.e. 0.001 µF at CB12 and CB13) if desired. Traces connecting Vcc and ground should be wide (low impedance, not 50 Ohm dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB1, CB11, and CB21 if desired.

6.1.5 Sample Waveforms from the LVDS Evaluation PCB

Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals should swing between 1.0 V (V_{OL}) and 1.3 V (V_{OH}) for a 300 mV V_{OD}. The differential waveform is constructed by subtracting the B (inverting) signal from the A (true) signal. V_{OD} = A - B. The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in Figure #3.

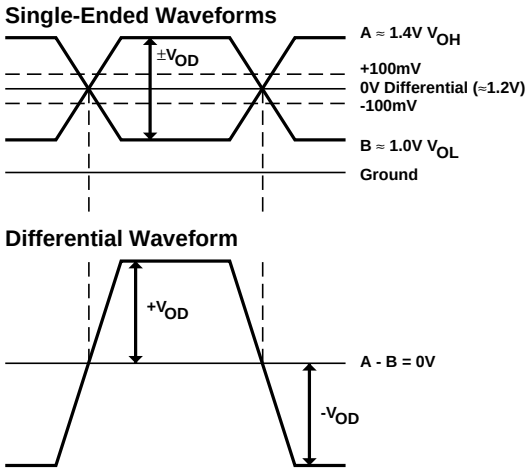


Figure 3: Single-ended & Differential Waveforms

The PCB interconnect signal (LVDS Channel #4) can be measured at the receiver inputs (test points A4 and B4). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See figure 4. Note that the data rate is 50 Mbps and the differential waveform (V_{DIFF}) shows fast transition times with little distortion.

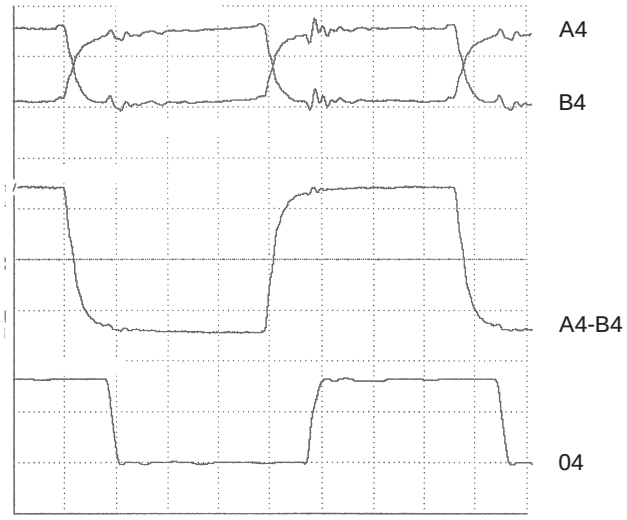


Figure 4: LVDS Channel #4 Waveforms — PCB Interconnect

The cable interconnect signal is also measured at the receiver inputs (test points A1 & B1 and A2 & B2). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with a SCSI-2 cable of 1 meter and also 2 meters in length are shown in figure 5 and 6. Note the additional transition time slowing due to the cable's filter effects on the 2 meter test case.

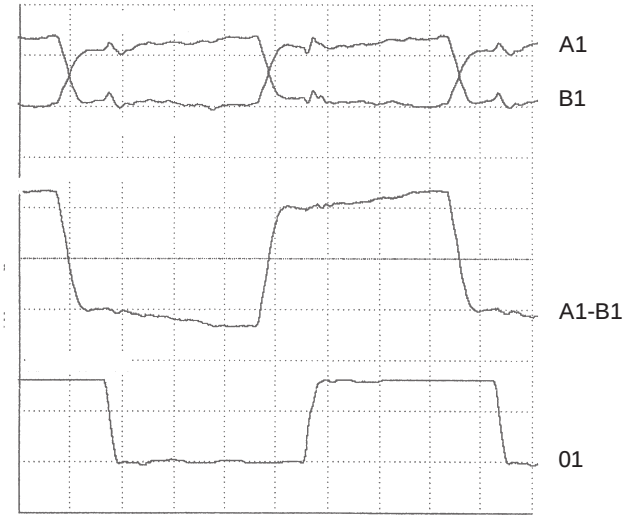


Figure 5: LVDS Channel #1 Waveforms - 1m Cable Interconnect

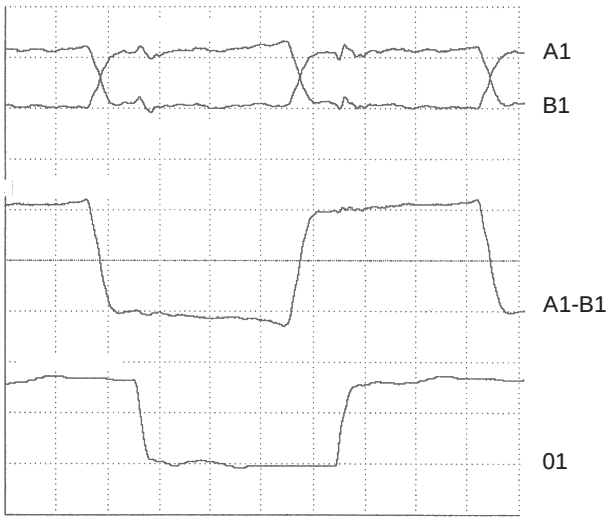


Figure 6: LVDS Channel #1 Waveforms - 2m Cable Interconnect

6.1.6 Probing of High Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). A high impedance probe must be used (100k Ohm or greater). The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 Ghz (4 Ghz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK 11801B scope (50 Ghz Bandwidth) and SD14 probe heads. These probes offer 100k Ohm, 0.4 pF loading and a bandwidth of 4 Ghz. This test equipment was used to acquire the waveforms shown in figures 4, 5 and 6.

LVDS waveforms may also be measured with lower bandwidth / different loading probes such as common TEK probes P6135A (150 MHz/1M Ohm / 10.5 pF). These probes were connected to a TEK 602 scope. See figure 7 for the LVDS waveforms acquired in this set up and compare these to figure 5. The waveform shows less DC loading (1M Ohm compared to 100k Ohm) and also more capacitive loading and band-width limiting. Probes with standard 50 Ohm loading should not be since they will load the LVDS signals too heavily. 50 Ohm probes may be used on the receiver output signal in conjunction the 450 Ohm series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50/(450 +50) or 1/10) of the output signal and the receiver output is loaded with 500 Ohm to ground.

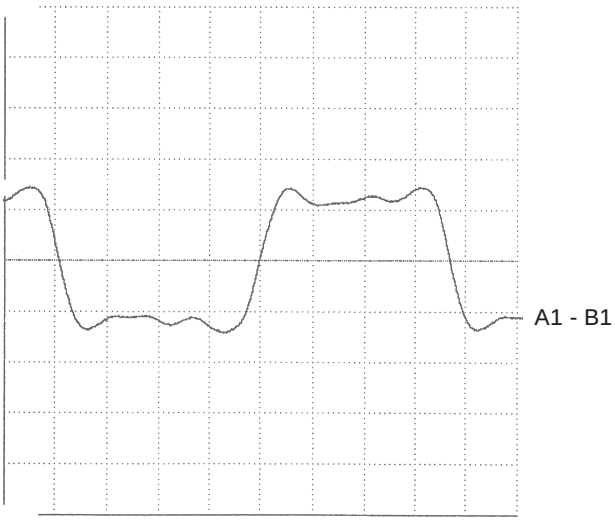


Figure 7: LVDS differential waveform measured with TEK P6135A probes and 602 scope

6.1.7 Demo PCB Options

Option 1: 450 Ohm Resistors

A provision for a series 450 Ohm resistor (RS1-4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 450 Ohm resistor a standard 50 Ohm scope probe may be used (500 Ohm total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver

The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J1). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the driver connect the jumper to ground, to disable the driver connect the jumper to the power plane.

Option 3: Disabling the LVDS Receiver

The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB the active high input has been hard wired to ground (-, off). The active low input (EN*) is routed to a jumper (J2). The jumper provides a connection to the Vcc plane (+) or to the Ground plane (-). To enable the receiver connect the jumper to ground, to disable the receiver connect the jumper to the power plane.

Option 4: Cables

Different cables may also be tested (different lengths, materials, constructions). A standard SCSI-2 50-pin connector/pinout has been used (J3 and J4). Simply plug in a SCSI-2 cable or build a custom cable.

Option 5: Power Supply /Components (C/LV/422)

The LVDS quads are offered in an industry standard pinout made popular by the 26LS31/2 quad 5V RS-422 devices. This standard pinout allows different devices (and power supplies) to be substituted and evaluated. The following National Semiconductor devices may be tested (U1/U2):

Devices (D/R)	Power Supply	Signaling Levels
DS90C031/2	5V	LVDS Signals
DS90LV031/2	3.3V	LVDS Signals
DS90LV031A/2A	3.3V	FAST LVDS (planned devices)
DS26C31/2A	5V	RS-422 Signals
DS26LV31/2A	3.3V	RS-422 Signals

Option 6: Receiver Termination (Channel #5)

The separate receiver input signals can be terminated separately (50 Ohm on each line to ground) utilizing pads RT5 (true input to ground) and RT6 (inverting to ground) for a signal generator interface. Or with a single 100 Ohm differential resistor (pad RL5) if the device is to be driven by a differential driver.

6.1.8 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

1) Connect signal common (Ground) to the black binding post

2) Connect the power supply lead to the red binding post (5V or 3.3V)

3) Set J1 & J2 jumpers to ground (-) to enable the drivers and receivers

4) Connect a signal generator to the driver input (I4) with:

   a) frequency = 50 Mhz (100 Mbps)

   b) V_{IL} = 0V & V_{IH} = 3.0V

   c) t_r & t_f = 2 ns

   d) duty cycle = 50% (square wave)

5) Connect high impedance probes to test points A4 and B4

6) View LVDS signals using the same voltage offset and volts/div settings on the scope with high impedance probes. View the output signal on a separate channel from test point O4.

6.1.9 Common Mode Noise

When the receivers (DS90C032, DS90LV032) are enabled common mode noise is passed from the output of the receiver to the inputs. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. For improved signal fidelity a design improvement is under way to reduce the magnitude of the noise coupled back to the inputs. This noise will not be observed if the receiver device is disabled by setting J2 to “+”.

6.1.10 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for data transmission applications.

6.1.11 Appendix

Typical test equipment used for LVDS measurements:

Signal Generator	TEK HFS 9009
Oscilloscope	TEK 11801B
Probes	TEK SD-14

Bill of Materials

Type	Label	Value / Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L SOIC	DS90LV031TM or other
IC	U2	(Quad Receiver)	1	16-L SOIC	DS90LV032TM or other
Connector	J3, J4	(50 pin SCSI-2)	2		AMP P/N 749721-5
Resistor	RT1-4	50 Ohm	4	RC0805	
Resistor	RL1-5	100 Ohm	5-Apr	RC0805	
Resistor	RS1-4	450 Ohm	0/4	RC0805	
Capacitor	CB2, CB3	0.1 uF	2	CC0805	
Capacitor	CB12, CB13	0.001 uF	0/2	CC0805	
Capacitor	CBR1	10 uF, 16V	1	CAP100RP	Electrolytic Radial Lead
Capacitor	CB1/11/21	na	0/3	CC0805	
Jumper Stakes	J1, J2x	3 STAKES	2		100 mil spacing
Jumpers	-		2		
SMB Jack	-		18	SMB Connector	Labels: I1-4, A1-5, B1-5, O1-2, O4-5. EF Johnson P/N 131-1701-201
Plug		Binding Post	2		Superior Electronic P/N BP21R, BP21B (1 each)
Cable	na	SCSI-2 type A Cable	0/1		
Legs			4		
bolts/washers			4		
PCB			1		LVDSEVAL-001 or LIT#550061-001

Reference and Fax Feedback Form

Chapter 7

7.0.0 REFERENCE AND CONTACT INFORMATION

7.1.0 APPLICATION NOTES

The list of additional application information about LVDS is growing. Following is a list of application notes at press time. The 1996 Interface Databook (literature number 400045) contains much information, but is now outdated. Up-to-date information can be retrieved from our Website.

	AN#	Title	Databook[1]	Web[2]
LVDS	AN-971	An Overview of LVDS Technology	•	•
	AN-977	LVDS Signal Quality: Jitter Measurements Using Eye Pattern	•	•
	AN-1035	PCB Design Guidelines for LVDS Technology	•	•
	AN-1040	Bit Error Rate (BER) Testing Data		•
	AN-1060	EDN Article Reprint (1/97)		•
Channel & FPD Links	AN-1032	An Introduction to FPD Link	•	•
	AN-1041	Channel Link Introduction		•
	AN-1045	FPD Rising/Falling Edge Clocking and Bit Mapping		•
	AN-1056	FPD STN Panel Applications		
	AN-1059	Skew and Jitter		
General	AN-806	Data Transmissions Lines and Their Characteristics	•	•
	AN-807	Reflections:Computations & Waveforms	•	•
	AN-808	Long Transmission Lines & Data Signal Quality	•	•
	AN-905	Transmission Line Rapidesigner Operations[3]		•
	AN-912	Common Data Transmission Parameters & Their Definitions	•	•
	AN-916	A Practical Guide To Cable Selection	•	•
	Sect. 13	IBIS Simulation Model Information	•	

[1]The literature number for the Interface Databook is Lit# 400045

[2] National's Web address is http://www.national.com

[3] The literature number for the Transmission Line Rapidesigner is Lit# 633200-001 (metric) or 633201-001 (English units). (The accompanying application note, AN-905, is also available separately as Lit# 100905-001)

7.2.0 ANSI/TIA/EIA-644 STANDARD

To order copies of the ANSI/TIA/EIA-644 Standard contact:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704

or call

USA and Canada: 1.800.854.7179
International: 1.303.397.7956

7.3.0 IBIS I/O MODEL INFORMATION

I/O Buffer Information Specification (IBIS) is a behavioral model specification defined within the ANSI/EIA-656 standard. LVDS IBIS models are available from National's Website which can be used by almost any simulators/EDA tools in the industry.

Visit the ANSI/EIA-656 Website: **www.eia.org/EIG/IBIS/ibis.htm** for a vendor listing or contact your software vendor. Chapter 13 of National's 1996 Interface Databook (lit#400045) describes IBIS models in detail.

Two sets of IBIS models (DS90C031/032 and DS90LV031/032) can represent the LVDS I/O characteristics of most of National's LVDS devices.

a) Use the DS90C031/032 models to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.

b) Use the DS90LV031/032 models to represent the LVDS I/O characteristics of the DS90LV031/032/017/027 devices.

c) Use the DS36C200 model for the DS36C200.

d) Contact National for availability of models to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices not listed in (b) above.

National IBIS models are available at: **www.national.com/models/ibis/ibis.html**

LVDS Fax Feedback

To: **National Semiconductor LVDS Marketing**

Fax: **1.408.737.7218**

From:

Mr./Ms.	Last Name	First Name	Title
Company		Dept./Division	
Address		Mail Stop	
City		State	Zip/Country
Phone	Ext.	Fax	
Email address			

The LVDS Owner's Manual Design Guide is (check one):

❑ Excellent ❑ Good ❑ Average ❑ Poor

Comments and suggestions for improvement:

_____
_____
_____
_____

I am interested in the following LVDS products (check all that apply):

❑ Drivers/Receivers ❑ Channel Link ❑ FPD-Link ❑ Other

New product suggestions:

_____
_____
_____
_____

My application is: _____

Please call me regarding LVDS in my application (check one): ❑ Yes ❑ No

Other comments:

_____
_____
_____
_____
_____

Thank you for your feedback, it is important to us!

Index & Worldwide Sales Offices

Chapter 8

APPENDIX E

National Semiconductor

LVDS Owner's Manual

A General Design Guide for National's Low Voltage Differential Signaling (LVDS) and Bus LVDS Products

Moving Info with LVDS

2nd Edition

Revision 2.0 — Spring 2000

LVDS Owner's Manual

Table of Contents

Introduction to LVDS

Chapter 1

1.0.0 INTRODUCTION TO LVDS

LVDS stands for Low Voltage Differential Signaling. It is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces or a balanced cable.

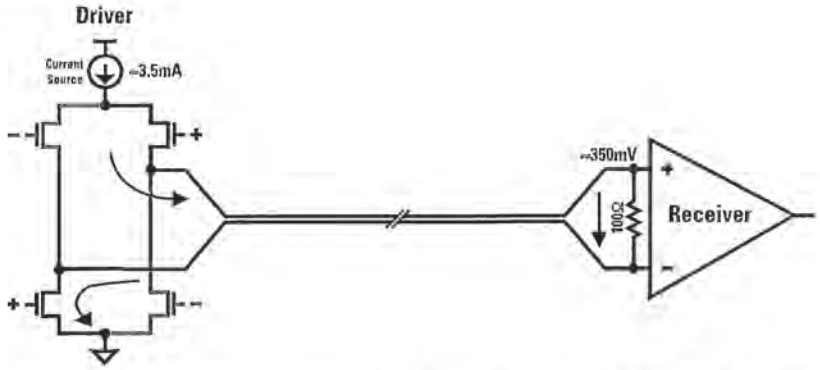
1.1.0 THE TREND TO LVDS

Consumers are demanding more realistic, visual information in the office and in the home. This is driving the need to move video, 3-D graphics and photo-realistic image data from camera to PCs and printers through LAN, phone, and satellite systems to home set top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances: on a printed circuit board (PCB) and across fiber or satellite networks. Moving this data from board-to-board or box-to-box, however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise (must meet increasingly stringent FCC/CISPR EMI requirements), is relatively immune to noise and is inexpensive. Unfortunately existing solutions are a compromise of these four basic ingredients: **performance, power, noise, and cost.**

1.2.0 GETTING SPEED WITH LOW NOISE AND LOW POWER

LVDS is a low swing, differential signaling technology which allows single channel data transmission at hundreds or even thousands of Megabits per second (Mbps). Its low swing and current-mode driver outputs create low noise and provide very low power consumption across frequency.

1.2.1 How LVDS Works



Simplified Diagram of LVDS Driver and Receiver Connected via 100Ω Differential Impedance Media

National's LVDS outputs consist of a current source (nominal 3.5mA) which drives the differential pair line. The basic receiver has high DC input impedance, so the majority of driver current flows across the 100Ω termination resistor generating about 350mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 Why Low Swing Differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. And, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low — almost flat — power consumption across frequency is obtained. Switching spikes in the driver are very small, so that I_{CC} does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5mA x 350mV = 1.2mW) is very small in magnitude.

1.2.3 The LVDS Standard

LVDS is currently standardized by two different standards:

TIA/EIA (Telecommunications Industry Association/Electronic Industries Association)
- ANSI/TIA/EIA-644 (LVDS) Standard

IEEE (Institute for Electrical and Electronics Engineering)
- IEEE 1596.3

The generic (multi-application) LVDS standard, **ANSI/TIA/EIA-644**, began in the TIA Data Transmission Interface committee TR30.2. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644 is intended to be reference by other standards that specify the complete interface (connectors, protocol, etc.). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644 (LVDS) Standard
Note: Actual datasheet specifications may be significantly better.

Parameter	Description	Min	Max	Units
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	|mV|
ΔV_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short Circuit Current		24	|mA|
t_r/t_f	Output Rise/Fall Times (≥200Mbps)	0.26	1.5	ns
	Output Rise/Fall Times (<200Mbps)	0.26	30% of t_{ui}†	ns
I_{IN}	Input Current		20	|μA|
V_{TH}	|Threshold Voltage|		±100	mV
V_{IN}	Input Voltage Range	0	2.4	V

† t_{ui} is unit interval (i.e. bit width).

The ANSI/TIA/EIA standard notes a recommend a maximum data rate of 655Mbps (based on one set of assumptions) and it also provides a theoretical maximum of 1.923Gbps based on a loss-less medium. This allows the referencing standard to specify the maximum data rate required depending upon required signal quality and media length/type. The standard also covers minimum media specifications, failsafe operation of the receiver under fault conditions, and other configuration issues such as multiple

receiver operation. The ANSI/TIA/EIA-644 standard was approved in November 1995. National Semiconductor held the editor position for this standard and chairs the sub committee responsible for electrical TIA interface standards. Currently the 644 spec is being revised to include additional information about multiple receiver operation. The revised (to be known as TIA-644-A) is expected to be balloted upon in calendar year 2000.

The other LVDS standard is from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the IEEE 1596.3 standard. The SCI-LVDS standard also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644 standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996. National Semiconductor chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

1.2.4 A Quick Comparison between Differential Signaling Technologies

Parameter	RS-422	PECL	LVDS
Differential Driver Output Voltage	±2 to ±5 V	±600-1000mV	±250-450mV
Receiver Input Threshold	±200mV	±200-300mV	±100mV
Data Rate	<30Mbps	>400Mbps	>400Mbps

Parameter	RS-422	PECL	LVDS*
Supply Current Quad Driver (no load, static)	60mA (max)	32-65mA (max)	8.0mA
Supply Current Quad Receiver (no load, static)	23mA (max)	40mA (max)	15mA (max)
Propagation Delay of Driver	11ns (max)	4.5ns (max)	1.7ns (max)
Propagation Delay of Receiver	30ns (max)	7.0ns (max)	2.7ns (max)
Pulse Skew (Driver or Receiver)	N/A	500ps (max)	400ps (max)

*LVDS devices noted are DS90LV047A/048A

The chart above compares basic LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are one-tenth of RS-422 and also traditional TTL/CMOS levels. Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

1.2.5 Easy Termination

Whether the LVDS transmission medium consists of a cable or controlled impedance traces on a printed circuit board, the transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides the optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cable or PCB traces differential impedance. Commonly 100Ω media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL can require more complex termination than the one-resistor solution for LVDS. PECL drivers commonly require 220Ω pull down resistors from each driver output, along with 100Ω resistor across the receiver input.

1.2.6 Maximum Switching Speed

Maximum switching speed of a LVDS Interface is a complex question, and its answer depends upon several factors. These factors are the performance of the Line Driver (Edge Rate) and Receiver, the bandwidth of the media, and the required signal quality for the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS (i.e. DS90LV047A)

2. Bandwidth performance of the selected media (cable) – type and length dependent

In the case of LVDS drivers, like the DS90LV047A, its speed is limited by how fast the TTL data can be delivered to the driver.

National's Channel Link devices capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream — more about this later.

1.2.7 Saving Power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination, for 90mW power consumption — 75 times more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices (quad device comparison).

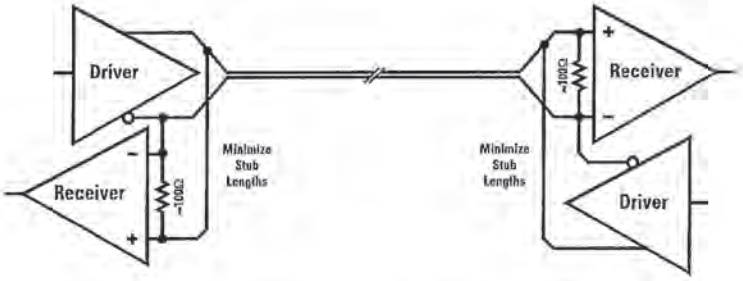
Aside from the power dissipated in the load and static I_{CC} current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of I_{CC}. The I_{CC} vs. Frequency plot for LVDS is virtually flat between 10MHz and 100MHz for the quad devices (DS90C031/2), <50mA total for driver and receiver at 100MHz. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

1.2.8 LVDS Configurations

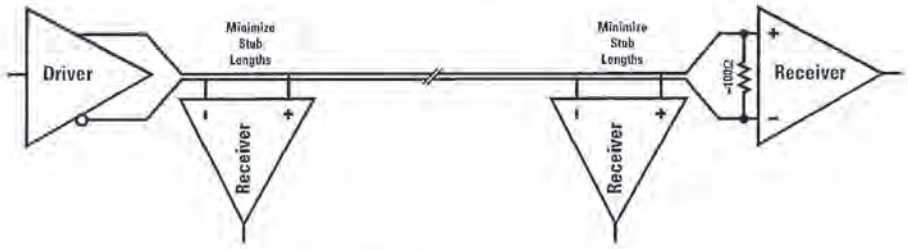
Point-to-Point Configuration

LVDS drivers and receivers are commonly used in a point-to-point configurations as shown above. However, other topologies/configurations are also possible.

The configuration shown next allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (<10m). (See also Bus LVDS Devices (Chapter 6) - which are designed for double termination loads and provide full LVDS compatible levels).



Bi-Directional Half-Duplex Configuration



Multidrop Configuration

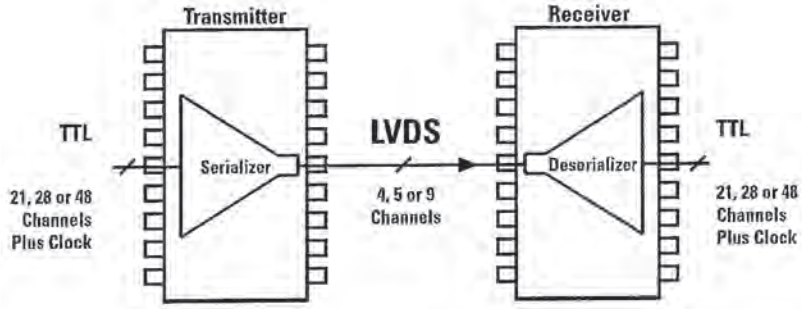
A multidrop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than12mm – application dependent). (See also Bus LVDS Devices, which are designed for double termination loads and provide LVDS compatible levels)

Dedicated point-to-point links provide the best signal quality due to the clear path they provide. LVDS has many advantages that make it likely to become the next famous data transmission standard for data rates from DC to hundreds of Mbps and short haul distances in the tens of meters. In this role, LVDS will far exceed the 20Kbps to 30Mbps rates of the common RS-232, RS-422, and RS-485 standards.

1.3.0 AN ECONOMICAL INTERFACE - SAVE MONEY TOO

LVDS can save money in several important ways:

1. National's LVDS solutions are inexpensive CMOS implementations as compared to custom solutions on elaborate processes.
2. High performance can be achieved using low cost, off-the-shelf CAT3 cable and connectors, and/or FR4 material.
3. LVDS consumes very little power, so power supplies, fans, etc. can be reduced or eliminated.
4. LVDS is a low noise producing, noise tolerant technology – power supply and EMI noise headaches are greatly minimized.
5. LVDS transceivers are relatively inexpensive and can also be integrated around digital cores providing a higher level of integration.
6. Since LVDS can move data so much faster than TTL, multiple TTL signals can be serialized or mux'ed into a single LVDS channel, reducing board, connector, and cable costs.



National's Channel Link Chipsets Convert a TTL Bus into a Compact LVDS Data Stream and Back to TTL.

In fact, in some applications, the PCB, cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic (user-friendly) system.

1.4.0 LVDS APPLICATIONS

The high-speed and low power/noise/cost benefits of LVDS broaden the scope of LVDS applications far beyond those for traditional technologies. Here are some examples:

PC/Computing	Telecom/Datacom	Consumer/Commercial
Flat panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/controls
Digital Copiers		
System clustering	(Box-to-box & rack-to-rack)	
Multimedia peripheral links		

1.5.0 NATIONAL'S WIDE RANGE OF LVDS SOLUTIONS

National Semiconductor offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV047A/DS90LV048A quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains singles, duals and quad footprints.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI) devices. These parts provide a high bandwidth, low power, small size, low power interface enabling XGA/SXGA/UXGA and beyond displays for notebook and monitor applications.

Another more generalized use of LVDS is in the National Channel Link family, which can take 21, 28 or 48-bits of TTL data and converts it to 3, 4 or 8 channels of LVDS data plus LVDS clock. These devices provide fast data pipes (up to 5.4 Gbps throughput) and are well suited for high-speed network hubs or routers applications or anywhere a low cost, high-speed link is needed. Their serializing nature provides an overall savings to system cost as cable and connector physical size and cost are greatly reduced.

Bus LVDS is an extension of the LVDS Line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide

LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A 10-bit Serializer and Deserializer family of devices is available that embeds and recovers clock from a single serial stream. This chip set also provides a high level of integration with on-chip clock recovery circuitry. Certain Deserializers provide a random data lock capability (An Industry First). The Deserializer can be hot-plugged into a live data bus and does not require PLL training.

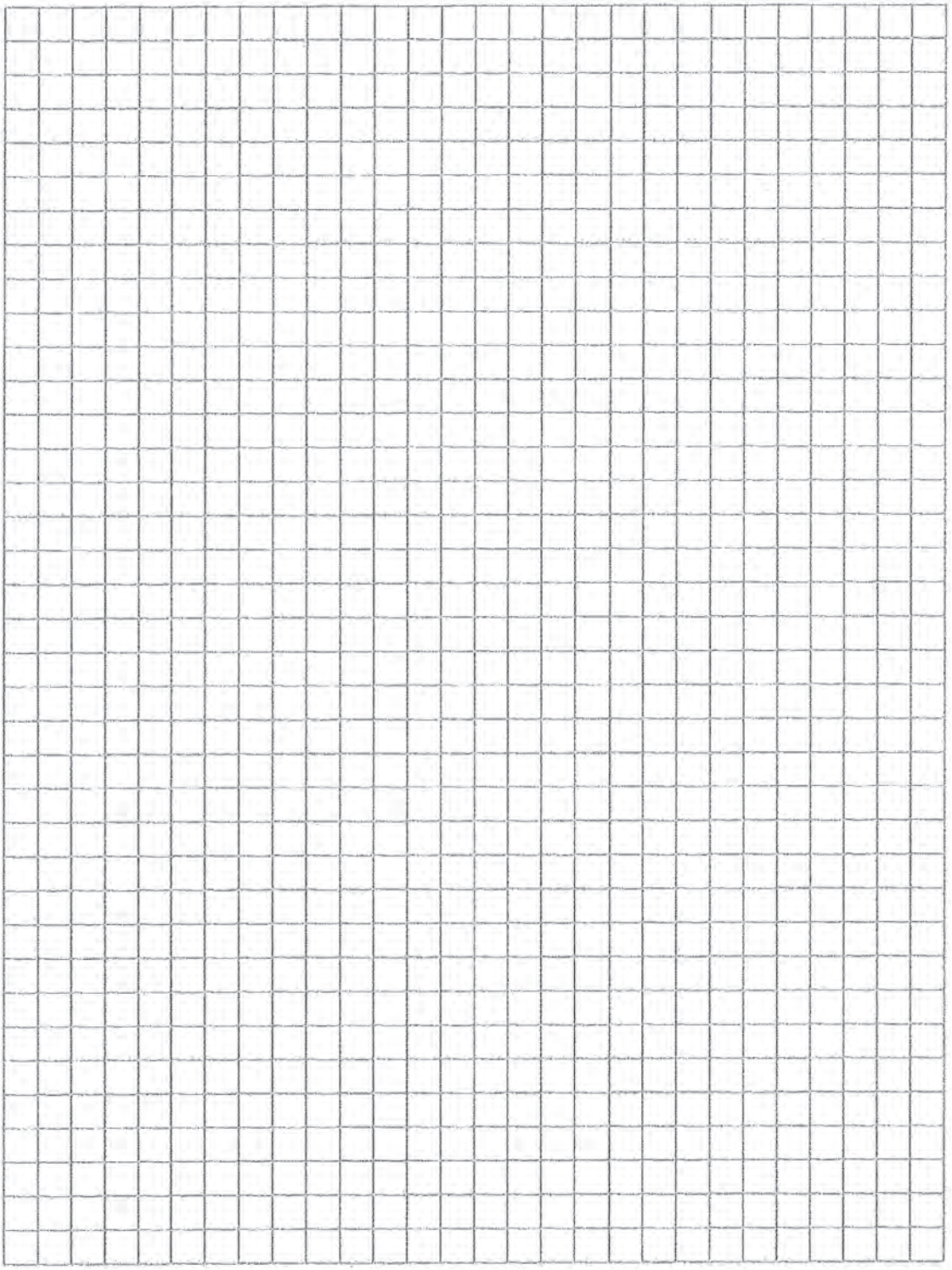
Special Functions are also being developed using LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs is available (DS92CK16) and also a line of crosspoint switches is being introduced.

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: **www.national.com/appinfo/lvds/**

1.6.0 CONCLUSION

National's LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

NOTES



LVDS Advantages

Chapter 2

2.0.0 LVDS ADVANTAGES

2.1.0 LVDS ELECTRICAL CHARACTERISTICS

LVDS current-mode, low-swing outputs mean that LVDS can drive at high-speeds (up to several hundred or even thousands of Mbps over short distances). If high-speed differential design techniques are used, signal noise and electromagnetic interference (EMI) can also be reduced with LVDS because of:

1. The low output voltage swing (≈350mV)
2. Relatively slow edge rates, dV/dt ≈ 0.300V/0.3ns = 1V/ns
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. "Soft" output corner transitions
5. Minimum I_{CC} spikes due to low current-mode operation

LVDS can be designed using CMOS processes, allowing LVDS to be integrated with standard digital blocks. LVDS can be used in commercial, industrial, and even military temperature ranges and operate from power supplies down to 2 volts. LVDS uses common copper PCB traces and readily available cables and connectors as transmission media, unlike fiber optics.

Presently the major limitations of LVDS are its point-to-point nature (as opposed to multipoint – see Bus LVDS) and short transmission distance (10-15m), where other technologies must presently be used.

Advantages	LVDS	PECL	Optics	RS-422	GTL	TTL
Data rate up to 1Gbps	+	+	+	-	-	-
Very low skew	+	+	+	-	+	-
Low dynamic power	+	-	+	-	-	-
Cost effective	+	-	-	+	+	+
Low noise/EMI	+	+	+	-	-	-
Single power supply/reference	+	-	+	+	-	+
Migration path to low voltage	+	-	+	-	+	+
Simple termination	+	-	-	+	-	+
Wide common-mode range	-	+	+	+	-	-
Process independent	+	-	+	+	+	+
Allows integration w/digital	+	-	-	-	+	+
Cable breakage/splicing issues	+	+	-	+	+	+
Long distance transmission	-	+	+	+	-	-
Industrial temp/voltage range	+	+	+	+	+	+

2.2.0 LVDS DRIVERS & RECEIVERS

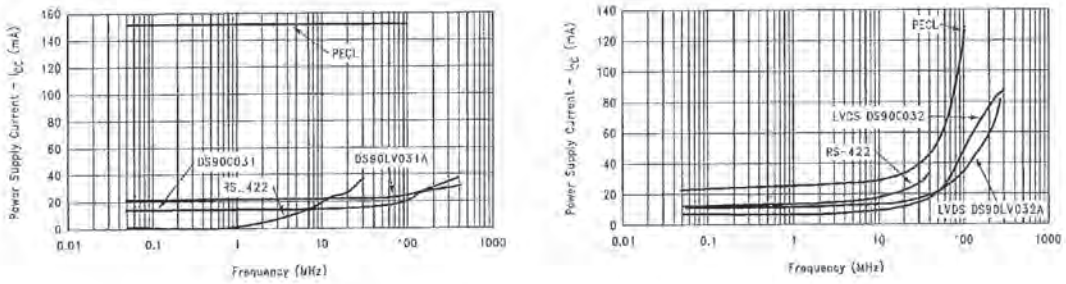
The most basic LVDS devices are the driver and receiver. These translate TTL to LVDS and back to TTL.

LVDS Drivers and Receivers Convert TTL to LVDS and Back to TTL.

Drivers and receivers transmit high-speed data across distances up to 10m with very low power, noise and cost.

Parameter	LVDS	PECL	Optics	RS-422	GTL	TTL
Output voltage swing	±350mV	±800mV	n/a	±2V	1.2V	2.4V
Receiver threshold	±100mV	±200mV	n/a	±200mV	100mV	1.2V
Speed (Mbps)	>400	>400	>1000	<30	<200	<100
Dynamic power	Low	High	Low	Low	High	High
Noise	Low	Low	Low	Low	Med	High
Cost	Low	High	High	Low	Low	Low

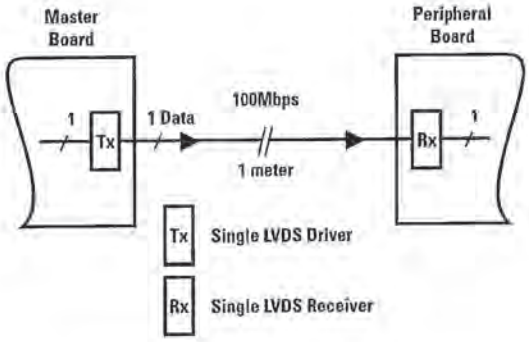
The table above summarizes that only LVDS can deliver the high-speed, ultra-low power, and low cost without compromise. PECL and ECL are expensive and consume too much power. TTL/CMOS is cheap, but is noisy and burns a lot of power at high-speeds. Fiber optics are expensive and have cables and connectors which are hard to manage.



I_{CC} vs. Frequency for 5V DS90C031/032 LVDS, 41LG/LF PECL, and 26C31/32 RS-422 Devices.

2.2.1 100Mbps Serial Interconnect

LVDS drivers and receivers are generally used to create serial or pseudo-serial point-to-point interconnects from 1Mbps to >400Mbps per channel. The following example summarizes the total performance and cost advantages of using LVDS over PECL or TTL for a serial 100Mbps 1 meter point-to-point link. Significantly higher data rates can be achieved for LVDS and PECL.



100Mbps Board-to-Board Link

100Mbps Serial Bitstream

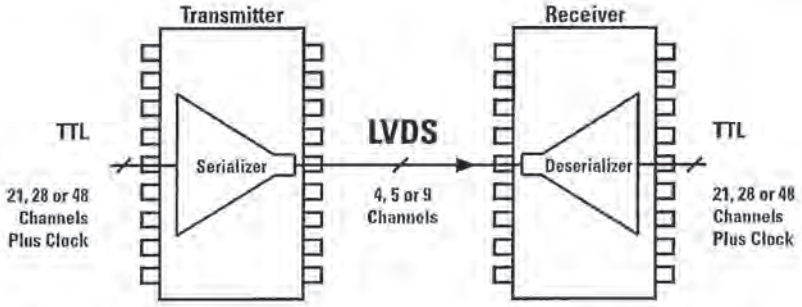
Performance Estimate				
Characteristic	**Parameter**	**LVDS**	**TTL**	**PECL**
Speed	Application Data Rate (Mbps)	100	100	100
	Max Capability per Channel (Mbps)	400	100	400
Power Consumption	Dynamic (mA) (@ 50MHz)	Low	High	Medium
	Static (mA)	8	10	48
Noise	Low EMI	+++	---	++
	Low Bounce	+++	---	++
Relative System Cost	**Total**	**4.05**	**3.30**	**6.10**
Cost Estimate				
Subsystem	**Parameter**	**LVDS**	**TTL**	**PECL**
General	Single-Ended or Differential	Differential	Single-Ended	Differential
	TTL Bus Width	1	1	1
	TTL Bus Speed (MHz)	50	50	50
	# Master Boards	1	1	1
	# Slave Boards	1	1	1
Transceivers	Description	DS90LV017A/018A	74LVT125	10ELT20/21
	# Drivers/Board (Master Board)	1	1	1
	# Rec/Board (Peripheral Board)	1	1	1
	Unit Cost	0.70	0.55	2.00
	Silicon Cost per Board	1.40	1.10	4.00
Termination	Voltage	None	None	None
	# Termination Regulators	0	0	0
	Unit Cost	0.00	0.00	0
	# Termination Resistors	1	2	2
	Unit Cost	0.05	0.05	0.05
	# Termination Capacitors	0	0	0
	Unit Cost	0.00	0.00	0.00
	Total Termination Cost	0.05	0.10	0.10
Transmission Medium	Cable Type	2 Pair CAT3	2 Pair CAT3	2 Pair CAT3
	Distance	1m	1m	1m
	#Conductors	2	2	2
	#Cables	1	1	1
	Connector Type	4-pin Wire to Board	4-pin Wire to Board	4-pin Wire to Board
	Unit Cable+Connector Assembly Cost	2.00	2.00	2.00
	Total Media Cost	2.00	2.00	2.00
Total Relative System Cost		**3.45**	**3.20**	**6.10**

Performance and Cost Estimates

The preceding example shows that LVDS provides a high-speed link with minimal noise, power, and cost. LVDS also creates an easy migration path to higher speeds, lower supply voltages, and higher integration that the other do not.

2.3.0 LVDS CHANNEL LINK SERIALIZERS

The speed of the LVDS line drivers and receivers is limited by how fast the TTL signals can be switched. Therefore, National has introduced a family of Channel Link serializers and deserializers. Instead of using one LVDS channel for every TTL channel, the Channel Link devices send multiple TTL channels through every LVDS channel thereby matching the speed of LVDS to that of TTL.



National's Channel Link Serializers/Deserializers can Dramatically Reduce the Size (and Cost) of Cables and Connectors.

Using fewer channels to convey data also means power and noise can be lower. The biggest advantage, however, is the significant reduction of cable and connector size. Since cables and connectors are usually quite expensive compared to silicon, dramatic cost savings can be achieved. Channel Link chipsets reduce cable size by up to 80%, reducing cable costs by as much as 50%. Plus, smaller cables are more flexible and user-friendly.

LVDS Channel Link serializer/deserializer devices take the inherent high-speed low power, noise, and cost advantages of LVDS and capitalize on the slow speed of TTL to generate significant benefits. For a small increase in silicon cost, Channel Link products can dramatically reduce total system costs and improve total system performance. Therefore, the total system should be evaluated if the true advantages are to be quantified. The following sections summarizes the cost and performance benefits of using Channel Link devices.

2.2.1 1Gbps 16-bit Interconnect

National's Channel Link serializers/deserializers take the benefits of LVDS (high-speed and low power, noise, and cost) and add serialization to further reduce cable, connector, and PCB size and cost. Channel Link is a great solution for high-speed data bus extension when the overhead of protocols is not desired. The following example compares the total performance and cost of moving a 16-bit 66MHz bus across 1 meter of cable using the 3V 66MHz 21-bit DS90CR215/216 Channel Link devices versus other solutions. Driving TTL signals over 1 meter of distance may be very risky due to the limited tolerance to noise (<400mV) and also transmission line problems generated by the TTL driver.

16-Bit Cable Interconnect

Performance Estimate

Characteristic	Parameter	Channel Link	TTL	GTL	ECL	Fibre Channel
Speed	Application Data Rate (Mbps)	1056	1056	1056	1056	1056
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 66MHz)	180	300	500	300	?
	Static (mA) (Outputs Disabled)	0.02 (Power Dn)	1	50	50	135
Noise	Low EMI	+++	- - -	- -	+	+++
	Low Bounce	+++	- - -	- -	++	+++
Ergonomics	Compact System Size	+++	- -	- -	- - -	+++
	Compact Transmission Medium Size	+++	-	+	+	+++
	Low Weight	+++	-	-	-	+++
Relative System Cost	Total	25.50	55.80	58.80	71.80	77.60

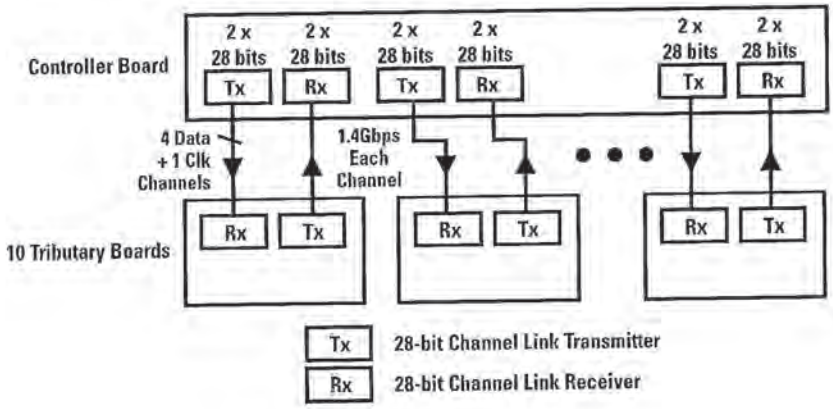
Cost Estimate

Subsystem	Parameter	Channel Link	TTL	GTL	ECL	Fibre Channel
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Differential	Differential ECL
	TTL Bus Width	16	16	16	16	16
	TTL Bus Speed (MHz)	66	66	66	66	66
	Multiplexed Scheme?	Yes	No	No	No	Yes
	# Master Boards	1	1	1	1	1
	# Slave Boards	1	1	1	1	1
Transceivers	Description	3V 21:4 Channel Link	ALVT 16-Bit	GTL 18-Bit	9-Bit Translators	Fibre Channel
	# Drivers/Board (Master Board)	1	1	1	2	1
	# Rec/Board (Peripheral Board)	1	1	1	2	1
	Unit Cost	3.70	2.40	3.25	5.00	20.00
	Silicon Cost per Board	7.40	4.80	6.50	20.00	40.00
PC Board	Layers	4	12	12	12	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	15.00	15.00	15.00	15.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	# Termination Regulators	0	0	1	1	1
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	# Termination Resistors	10	16	16	16	32
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	# Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	0.80	1.80	1.80	2.60
Transmission Medium	Cable Type	SCSI2 CAT3 Cable	Shielded Flat Cable	Shielded Flat Cable	SCSI2 CAT3 Cable	CAT5 Cable
	Distance	2m	2m	2m	2m	2m
	#Data+Clock Conductors	8	17	17	34	2
	#Power+Ground Conductors	4	10	10	15	2
	#Cables	1	1	1	1	1
	Connector Type	0.050 D - 20	D - 37	D - 37	0.050 D - 50	DB-9
	Unit Cable+Connector Assembly Cost	20.00	30.00	30.00	30.00	15.00
	Total Media Cost	15.00	30.00	30.00	30.00	15.00
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.3	1.2	1.2	1.2
	Total Add'l Power Supply Cost	0.00	5.00	5.00	5.00	5.00
Total Relative System Cost		22.90	55.60	58.30	71.80	77.60

Performance and Cost Estimates

2.2.2 1.4Gbps 56-Bit Backplane

In some large datacom and telecom systems, it is necessary to construct a very large, high-speed backplane. There is generally an inverse relationship between the size of a backplane and its maximum speed. In other words, if you try to make a backplane too large, the heavy loading will severely hamper backplane speed and make power and noise a big problem. Therefore, connecting or extending smaller backplanes via a high-speed cable interconnect is often the only solution. The previous examples illustrates how Channel Link may be used to accomplish this over cable. The cost benefits of using Channel Link to shrink cable and connector costs are clear. What would happen, however, if Channel Link were used to form or extend a backplane using a PCB as the medium. The following examples shows how Channel Link can reduce the size and number of layers of the printed circuit board transmission medium in the same way as Channel Link reduces the size and cost of cables.



1.4Gbps Backplane Using Point-to-Point Channel Links

56-Bit Backplane

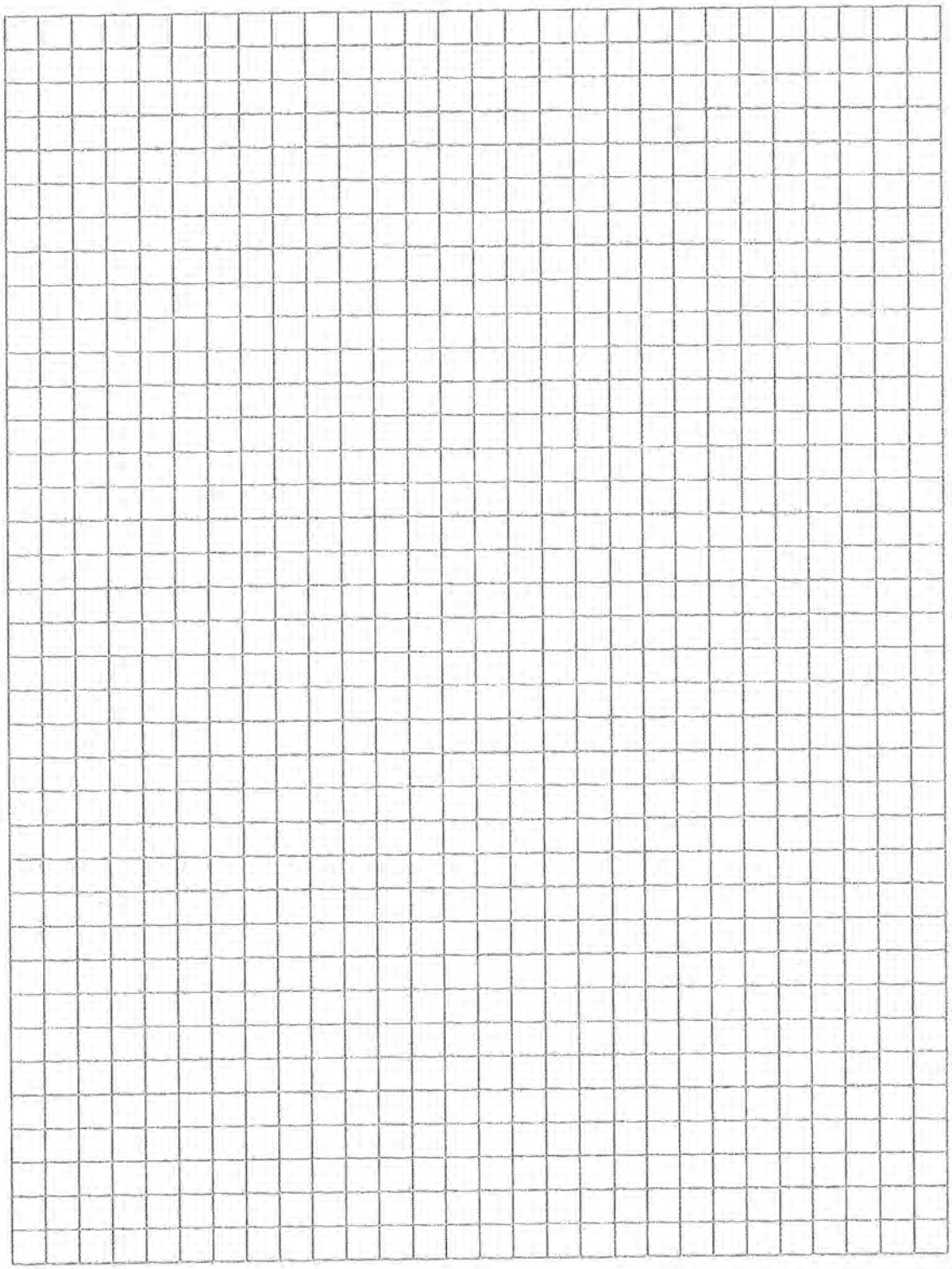
Performance Estimate						
Characteristic	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
Speed	Application Data Rate (Mbps)	1400	1400	1400	1400	1400
	Max Capability per Channel (Mbps)	462	100	150	800	800
Power Consumption	Dynamic (mA) (@ 50MHz)	2600	10000	6000	16000	?
(Loaded Tx/Rx's only)	Static (mA)	0.4 (Power on)	40	1840	3402	3818
Noise	Low EMI	+++	---	+	+	++
	Low Bounce	+++	---	+	+	++
Ergonomics	Compact System Size	++	+	+	+	++
	Compact Transmission Medium Size	++	-	+	+	++
	Fans?	No	No	No	Yes	Yes
	Low Weight	+++	-	-	-	+++
Relative System	Cost Per Board	51.05	66.12	75.04	191.04	574.22
	Total	510.50	661.20	750.40	1910.40	5742.20

Performance Estimate

Cost Estimate						
Subsystem	**Parameter**	**Channel Link**	**TTL**	**GTL/BTL**	**ECL**	**Fibre Channel**
General	Single-Ended or Differential	Differential	Single-Ended	Single-Ended	Single-Ended	Differential
	TTL Bus Width	56	56	56	56	56
	TTL Bus Speed (MHz)	50	50	50	50	50
	Multiplexed Scheme?	Yes	No	No	No	Yes
	Number Tributary Boards	10	10	10	10	10
	Number Channels in Link	10	56	56	56	14
	Number Conductors (Data)	20	56	56	56	28
	Number Conductors (CLK)	1	1	1	1	1
Transceivers	Description	28:5 Channel Link	LVT 16-Bit	GTL 18-Bit	9-Bit	Fibre Channel
	# Transceivers/Board (Trib Board)	4	4	4	14	14
	# Transceivers/Board (Ctrlr Board)	4	4	4	14	14
	Unit Cost	3.70	2.40	3.25	5.00	20.00
	Silicon Cost per Board	29.60	19.20	26.00	140.00	560.00
PC Board	Layers	12	26	26	26	12
	Size (Normalized)	1.15	1	1.15	15.63	11.97
	Total Additional PCB Cost	0.00	100.00	100.00	150.00	50.00
Termination	Voltage	None	None	1.5V	2.1V	3.0V
	Number Termination Regulators	0	0	14	14	14
	Unit Cost	0.00	0.00	1.00	1.00	1.00
	Number Termination Resistors	10	224	128	128	14
	Unit Cost	0.05	0.05	0.05	0.05	0.05
	Number Termination Capacitors	0	0	0	0	0
	Unit Cost	0.00	0.00	0.00	0.00	0.00
	Total Termination Cost	0.50	11.20	20.40	20.40	14.70
Transmission Medium	Type	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane	PCB Trace Backplane
	Distance	<1m	<1m	<1m	<1m	<1m
	Layers	12	26	26	26	12
	Size (Normalized)	1	1	1	1	1
	Number Media	1	1	1	1	1
	Additional Media Cost	0.00	200.00	200.00	200.00	0.00
	Total Add'l Trans. Media Cost	0.00	200.00	200.00	200.00	0.00
Connectors	Connector Type	Header	VME	VME	VME	Header
	Number Pins (Data+ CLK)	21	57	57	57	29
	Number Pins (Power/GND)	5	38	38	7	7
	Total Connector Pins	26	96	96	64	36
	Number Connector Pairs	1	1	1	1	1
	Cost of Pair	3.00	10.00	10.00	8.00	3.75
	Connector Cost per Board	3.00	10.00	10.00	8.00	3.75
Power Supply	Special Supply Voltages	0	0	1.5V	2.1V	3.0V
	Power Supply Size (Normalized)	1	1.5	1.5	1.7	1.4
	Total Add'l Power Supply Cost	0.00	50.00	50.00	60.00	40.00
Total Relative System Cost Per Board		49.21	66.64	74.84	191.04	574.22
Total Relative System Cost		492.10	666.40	748.40	1910.40	5742.20

Cost Estimate

NOTES



Selecting an LVDS Device/ LVDS Families

Chapter 3

3.0.0 SELECTING AN LVDS DEVICE

3.1.0 GENERAL

National is continually expanding its portfolio of LVDS devices. The devices listed below are current at the time this book goes to press. For the latest list of LVDS devices, please visit our LVDS website at: www.national.com/appinfo/lvds/

On this site, you will find the latest LVDS datasheets, application notes, selection tables, FAQs, modeling information/files, white papers, LVDS News, and much much more! The Web is constantly updated with new documents as they are available.

Application questions should be directed to your local National Semiconductor representative or to the US National Interface Hotline: 1-408-721-8500 (8 a.m. to 5 p.m. PST).

LVDS products are classified by device types. Please see below for a short description of each device type and selection table that was current at the time this edition of the LVDS Owner's Manual was printed. Again, visit our web site for the latest information.

3.1.1 Do I need LVDS?

If Megabits or Gigabits @ milliwatts are needed, then LVDS may be the answer for you! It provides high-speed data transmission, consumes little power, rejects noise, and is robust. It is ideal for interconnects of a few inches to tens of meters in length. It provides an ideal interface for chip-to-chip, card-to-card, shelf-to-shelf, rack-to-rack or box-to-box communication.

3.1.2 Which part should I use?

If point-to-point or multidrop configuration is needed – see the LVDS Line Driver/Receivers or Channel Link Family.

If multipoint or certain multidrop configurations are needed – then Bus LVDS offers the technology best suited for these applications.

Parallel? Serialize? Or Serial? – depends upon the application. Small busses typically use the simple PHY parts. However, if the bus is wide, then serialization may make the most sense. Serialization provides a smaller interconnect and reduces cable and connector size and cost. For this application, refer to the Channel Link and also the Bus LVDS SER/DES parts.

3.2.0 LVDS LINE DRIVERS & RECEIVERS

LVDS line drivers and receivers are used to convey information over PCB trace or cable if;

1. You only have a few channels of information to transmit, or
2. Your data is already serialized.

The following table summarizes National's LVDS line drivers and receivers. These devices are also referred to as simple PHYs.

LVDS Driver/Receiver/Transceiver Products

Order Number	# Dr.	# Rec.	Sup. Volt.	Temp	Speed per Channel	Typ I_{CC}@ 1Mbps (mA)	Max I_{CC} Disabled (mA)	Driver Max tpd (ns)	Driver Max Ch Skew (ns)	Receiver Max tpd (ns)	Receiver Max Ch Skew (ns)	Package	Comments
DS90LV047ATM	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16SOIC	
DS90LV047ATMTC	4	0	3.3	Ind	>400Mbps	20	6	1.7	0.5	—	—	16TSSOP	
DS90LV048ATM	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16SOIC	
DS90LV048ATMTC	0	4	3.3	Ind	>400Mbps	9	5	—	—	2.7	0.5	16TSSOP	
DS90LV031ATM	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16SOIC	
DS90LV031ATMTC	4	0	3.3	Ind	>400Mbps	21	6	2.0	0.5	—	—	16TSSOP	
DS90LV032ATM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16SOIC	
DS90LV032ATMTC	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.3	0.5	16TSSOP	
DS90LV031BTM	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16SOIC	Available soon
DS90LV031BTMTC	4	0	3.3	Ind	>400Mbps	22	6	2.0	0.5	—	—	16TSSOP	Available soon
DS90LV032BTM	0	4	3.3	Ind	>400Mbps	10	5	—	—	3.0	0.5	16SOIC	Available soon
DS90LV017ATM	1	0	3.3	Ind	>600Mbps	7	—	1.5	—	—	—	8 SOIC	
DS90LV017M	1	0	3.3	Com	>155Mbps	5.5	—	6.0	—	—	—	8 SOIC	
DS90LV018ATM	0	1	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	—	8 SOIC	
DS90LV019TM	1	1	3.3/5	Ind	>100Mbps	16/19	7/8.5	7.0/6.0	—	9.0/8.0	—	14 SOIC	
DS90LV027ATM	2	0	3.3	Ind	>600Mbps	14	—	1.5	0.8	—	—	8 SOIC	
DS90LV027M	2	0	3.3	Com	>155Mbps	9	—	6.0	—	—	—	8 SOIC	
DS90LV028ATM	0	2	3.3	Ind	>400Mbps	5.5	—	—	—	2.5	0.5	8 SOIC	
DS90LV031AW-QML	4	0	3.3	Mil	>400Mbps	21	12	3.6	1.75	—	—	16CERPAK	Mil spec
DS90C031TM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16SOIC	
DS90C032TM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	
DS90C031BTM	4	0	5	Ind	>155Mbps	15.5	4	3.5	1.0	—	—	16 SOIC	Pwr Off Hi-Z
DS90C032BTM	0	4	5	Ind	>155Mbps	5	10	—	—	6.0	1.5	16 SOIC	Pwr Off Hi-Z
DS90C031E-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	20 LCC	Military-883
DS90C032E-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	20 LCC	Military-883
DS90C031W-QML	4	0	5	Mil	>100Mbps	15.5	10	5.0	3.0	—	—	16Flatpack	Military-883
DS90C032W-QML	0	4	5	Mil	>100Mbps	5	11	—	—	8.0	3.0	16Flatpack	Military-883
DS90C401M	2	0	5	Ind	>155Mbps	4	—	3.5	1.0	—	—	8 SOIC	
DS90C402M	0	2	5	Ind	>155Mbps	4.5	—	—	—	6.0	1.5	8 SOIC	
DS36C200M	2	2	5	Com	>100Mbps	12	10	5.5	—	9.0	—	14 SOIC	1394 Link

Note: Evaluation boards utilize a quad driver/receiver pair to perform generic cable/PCB/etc LVDS driver/receiver evaluations, order number LVDS47/48EVK.

3.3.0 LVDS DIGITAL CROSSPOINT SWITCHES

For routing of high-speed point-to-point busses, crosspoint switches may be used. They are also very useful in applications with redundant backup interconnects for fault tolerance. This first device in this planned family of products is now available. It is a 2x2 Crosspoint that operates above 800Mbps and generates extremely low jitter.

LVDS Digital Crosspoint Switches

Order Number	Description	Supply Voltage	Speed	Number of Inputs	Number of Outputs	Package
DS90CP22M-8	2 x 2 800Mbps LVDS Crosspoint Switch	3.3V	800Mbps	2	2	16SOIC

3.4.0 LVDS CHANNEL LINK SERIALIZERS/DESERIALIZERS

If you have a wide TTL bus that you wish to transmit, use one of National's Channel Link devices. Channel Link will serialize your data for you, saving you money on cables and connectors and helping you avoid complex skew problems associated with a completely parallel solution. The following table summarizes National's Channel Link devices.

LVDS Channel Link Serializer/Deserializer Products

Order Number	Mux/Demux Ratio	Type	Supply Voltage	Clock Frequency	Max Throughput	Package	Comments	Eval Board Order Number
DS90CR211MTD	21:3	Transmitter	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR212MTD	21:3	Receiver	5	20-40MHz	840Mbps	48TSSOP		CLINK5V28BT-66
DS90CR213MTD	21:3	Transmitter	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR214MTD	21:3	Receiver	5	20-66MHz	1.38Gbps	48TSSOP		CLINK5V28BT-66
DS90CR215MTD	21:3	Transmitter	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216MTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP		CLINK3V28BT-66
DS90CR216AMTD	21:3	Receiver	3.3	20-66MHz	1.38Gbps	48TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR217MTD	21:3	Transmitter	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218AMTD	21:3	Receiver	3.3	20-85MHz	1.78Gbps	48TSSOP		See Note
DS90CR218MTD	21:3	Receiver	3.3	20-75MHz	1.575Gbps	48TSSOP		See Note
DS90CR281MTD	28:4	Transmitter	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR282MTD	28:4	Receiver	5	20-40MHz	1.12Gbps	56TSSOP		CLINK5V28BT-66
DS90CR283MTD	28:4	Transmitter	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR284MTD	28:4	Receiver	5	20-66MHz	1.84Gbps	56TSSOP		CLINK5V28BT-66
DS90CR285MTD	28:4	Transmitter	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286MTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP		CLINK3V28BT-66
DS90CR286AMTD	28:4	Receiver	3.3	20-66MHz	1.84Gbps	56TSSOP	Enhanced Set/Hold Times	CLINK3V28BT-66
DS90CR287MTD	28:4	Transmitter	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR288MTD	28:4	Receiver	3.3	20-75MHz	2.10Gbps	56TSSOP		See Note
DS90CR288AMTD	28:4	Receiver	3.3	20-85MHz	2.38Gbps	56TSSOP		See Note
DS90CR483VJD	48:8	Transmitter	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112
DS90CR484VJD	48:8	Receiver	3.3	32.5-112MHz	5.37Gbps	100TQFP		CLINK3V48BT-112

Note: 85MHz eval boards will be available in the future. For immediate needs, use CLINK3V28BT-66 with 75 or 85MHz parts.

3.5.0 LVDS FPD-LINK

Use National's FPD Link to convey graphics data from your PC or notebook motherboard to your flat panel displays. The next table summarizes National's FPD Link devices. This family has been extended with the LVDS Display Interface chipset that provides higher resolution support and long cable drive enhancements. The LDI Chipset is ideal for desktop monitor applications and also industrial display applications. The FPD-Link receiver function is also integrated into the timing controller devices to provide a small single-chip solution for TFT Panels.

LVDS Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI)

Order Number	Color Bits	Type	Supply Voltage	Max Clock Frequency	Clock Edge Strobe	Package	Comments	Eval Board Order Number
DS90CF561MTD	18-bit	Transmitter	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR561MTD	18-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF562MTD	18-bit	Receiver	5	40MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR562MTD	18-bit	Receiver	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CR581MTD	24-bit	Transmitter	5	40MHz	Rising	48TSSOP		FLINK5V8BT-65
DS90CF563MTD	18-bit	Transmitter	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR563MTD	18-bit	Transmitter	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF564MTD	18-bit	Receiver	5	65MHz	Falling	48TSSOP		FLINK5V8BT-65 *
DS90CR564MTD	18-bit	Receiver	5	65MHz	Rising	48TSSOP		FLINK5V8BT-65 *
DS90CF583MTD	24-bit	Transmitter	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR583MTD	24-bit	Transmitter	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90CF584MTD	24-bit	Receiver	5	65MHz	Falling	56TSSOP		FLINK5V8BT-65
DS90CR584MTD	24-bit	Receiver	5	65MHz	Rising	56TSSOP		FLINK5V8BT-65
DS90C363AMTD	18-bit	Transmitter	3.3	65MHz	Programmable	48TSSOP		FLINK3V8BT-65 *
DS90CF363AMTD	18-bit	Transmitter	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364MTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP		FLINK3V8BT-65 *
DS90CF364AMTD	18-bit	Receiver	3.3	65MHz	Falling	48TSSOP	50% CLKOUT	FLINK3V8BT-65 *
DS90C383AMTD	24-bit	Transmitter	3.3	65MHz	Programmable	56TSSOP		FLINK3V8BT-65
DS90CF383AMTD	24-bit	Transmitter	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384MTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP		FLINK3V8BT-65
DS90CF384AMTD	24-bit	Receiver	3.3	65MHz	Falling	56TSSOP	50% CLKOUT	FLINK3V8BT-65
DS90C365MTD	18-bit	Transmitter	3.3	85MHz	Programmable	48TSSOP		See Note *
DS90CF366MTD	18-bit	Receiver	3.3	85MHz	Falling	48TSSOP		See Note *
DS90C385MTD	24-bit	Transmitter	3.3	85MHz	Programmable	56TSSOP		See Note
DS90CF386MTD	24-bit	Receiver	3.3	85MHz	Falling	56TSSOP		See Note
DS90C387VJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP		LDI3V8BT-112
DS90C387AVJD	48-bit	Transmitter	3.3	112MHz	Programmable	100TQFP	Non-DC Balanced	NA
DS90CF388VJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP		LDI3V8BT-112
DS90CF388AVJD	48-bit	Receiver	3.3	112MHz	Falling	100TQFP	Non-DC Balanced	NA

* For 18-bit evaluation, use 24-bit board for evaluation purposes.
Note: 85MHz eval boards will be available in the future. For immediate needs, FLINK3V8BT-65 can be used with 85MHz part.

LVDS Flat Panel Display Timing Controller Products

Order Number	Color Bits	Resolutions Supported	Supply Voltage	Max Clock Frequency	TCON Core	Package	Input/Output	Eval Board Order Number
FPD85310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/TTL dual port output	Call
FPD87310VJD	6 or 8	XGA/SVGA	3.3	65MHz	Programmable	TQFP	LVDS input/RSDS single port output	Call

Note: FPD8710 in sampling phase.

3.6.0 BUS LVDS

Bus LVDS is an extension of the LVDS line drivers and receivers family. They are specifically designed for multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30 to 50Ω range. Bus LVDS drivers provide about 10mA of output current so that they provide LVDS swings with heavier termination loads. Transceivers and Repeaters are currently available in this product family. A "10-bit" Serializer and Deserializer family of devices is also available that embeds and recovers the clock from a single serial stream. This chipset also provides a high level of integration reducing complexity and overhead to link layer ASICs. Clock recovery and "Random Lock" digital blocks are integrated with the core interface line driving and receiving functions. The Deserializer (DS92LV1212/1224) can also be hot-plugged into a live data bus and does not require PLL training.

Special functions are also being developed using BLVDS/LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs (DS92CK16) and a Repeater/MUX with selectable drive levels (DS92LV222A) are available.

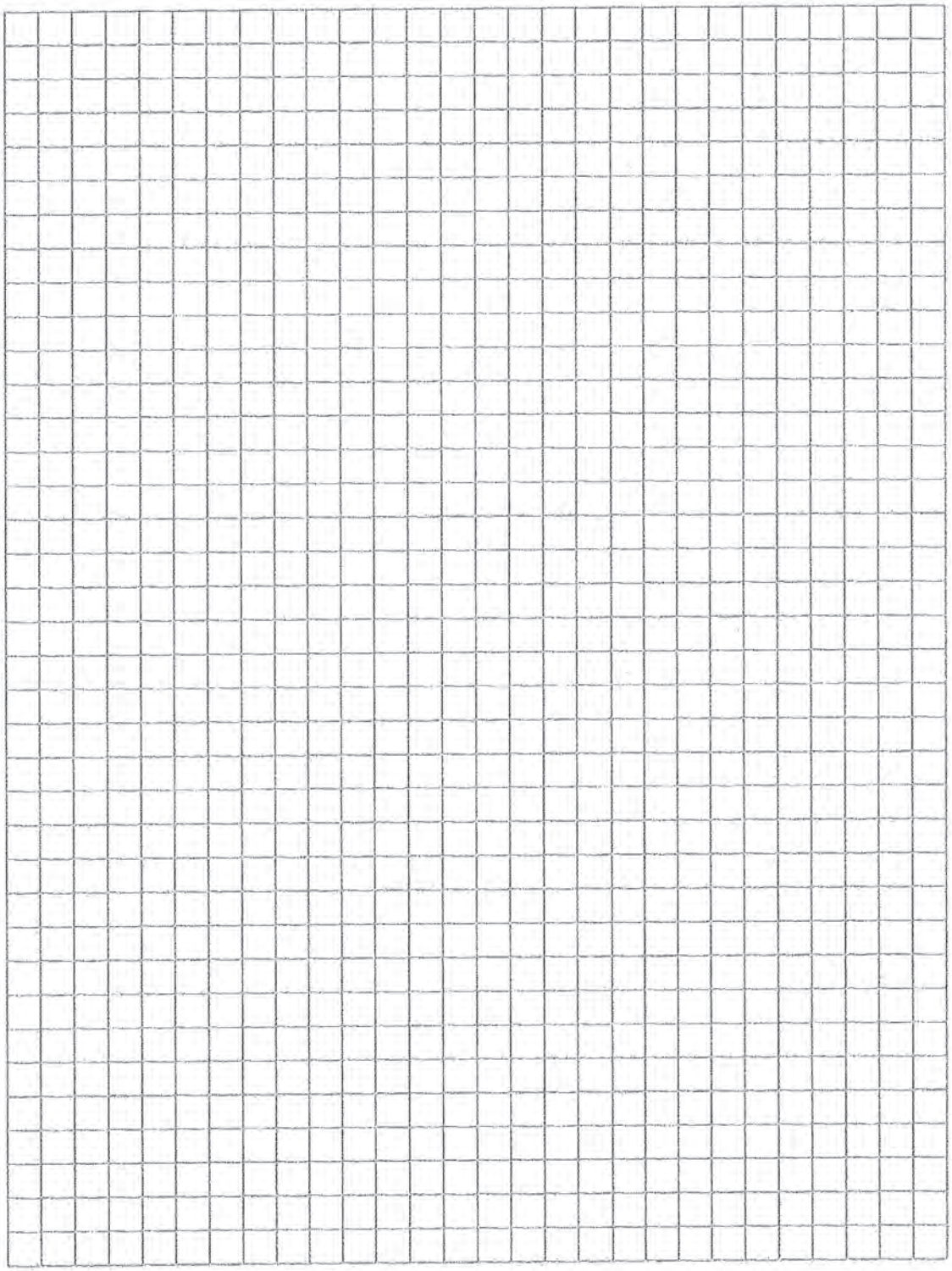
Bus LVDS Products

Order Number	Description	Supply Voltage	Speed	Features	Package
DS92LV010ATM	Single Bus LVDS Transceiver	3.3/5	155Mbps/Ch	3.3V or 5V Operation	8SOIC
DS92LV222ATM	Bus LVDS or LVDS Repeater/Mux	3.3	200Mbps/Ch	Repeater, Mux, or 1:2 Clock Driver Modes	16SOIC
DS92LV090ATVEH	9-Chennel Bus LVDS Transceiver	3.3	200Mbps/Ch	Low Part-to-Part Skew	64PQFP
DS92LV1021TMSA	10:1 Serializer w/Embedded Clock	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1210TMSA	1:10 Deserializer w/Clock Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1212TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	40MHz	400Mbps Data Payload Over Single Pair	28SSOP
DS92LV1023TMSA	10:1 Serializer w/Embedded Clock	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92LV1224TMSA	1:10 Random Lock Deserializer w/Clk Recovery	3.3	66MHz	660Mbps Data Payload Over Single Pair	28SSOP
DS92CK16TMTC	1:6 Clock Distribution	3.3	125MHz	50ps TTL output channel-to-channal skew	24TSSOP
More to come...					

3.7.0 SUMMARY

Over 75 different LVDS products are currently offered by National. For the latest in product information, and news, please visit National's LVDS web site at: www.national.com/appinfo/lvds/

NOTES



Designing with LVDS

Chapter 4

4.0.0 DESIGNING WITH LVDS

4.1.0 PCB BOARD LAYOUT TIPS

Now that we have explained how LVDS has super speed, and very low: power, noise, and cost, many people might assume that switching to LVDS (or any differential technology) will solve all of their noise problems. It will not, but it can help a lot! LVDS has low swing, differential, ~3.5mA current-mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond which means that every interconnect will act as a transmission line except the very shortest. Therefore, knowledge of ultra-high-speed board design and differential signal theory is required. Designing high-speed differential boards is not difficult or expensive, so familiarize yourself with these techniques before you begin your design.

Generalized Design Recommendations are provided next.

The edge rate of an LVDS driver means that impedance matching is very important even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI. You should use controlled differential impedance traces as soon as you can after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12mm (0.5in). Also, avoid 90° turns since this causes impedance discontinuities; use 45 turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs which looks like and radiates as common-mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are inexpensive and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should provide maximum performance and be quick and easy to develop.

4.1.1 PC Board

a) Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals. Dedicating planes for V_{CC} and Ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground can also create an excellent high frequency bypass capacitance.

b) Isolate fast edge rate CMOS/TTL signals from LVDS signals, otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. It is best to put TTL and LVDS signals on a different layer(s) which should be isolated by the power and ground planes.

c) Keep drivers and receivers as close to the (LVDS port side) connectors as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and escapes the board as EMI from the cable interconnect. This recommendation also helps to minimize skew between the lines. Skew tends to proportional to length, therefore by limiting length also limits skew.

d) Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power Supply: A 4.7µF or 10µF 35V tantalum capacitor works well between supply and ground. Choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 to 300MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} Pins: One or two multi-layer ceramic (MLC) surface mount capacitors (0.1µF and 0.01µF) in parallel should be used between each V_{CC} pin and ground if possible. For best results, the capacitors should be placed as close as possible to the V_{CC} pins to minimize parasitic effects that defeat the frequency response of the capacitance. Wide (>4-bits) and PLL-equipped (e.g. Channel Link & FPD-Link) LVDS devices should have at least two capacitors per power type, while other LVDS devices are usually fine with a 0.1µF capacitor. The bottom line is to use good bypassing practices. EMI problems many times start with power and ground distribution problems. EMI can be greatly reduced by keeping power and ground planes quiet.

e) Power and ground should use wide (low impedance) traces. Do not use 50Ω design rules on power and ground traces. Their job is to be a low impedance point.

f) Keep ground PCB return paths short and wide. Provide a return path that create the smallest loop for the image currents to return.

g) Cables should employ a ground return wire connecting the grounds of the two systems. This provides for common-mode currents to return on a short known path. See Chapter 5, Section 5.3.0

h) Use two vias to connect to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

4.1.2 Traces

a) Edge-coupled Microstrip, Edge-coupled Stripline, or Broad-side Striplines all work well for differential lines.

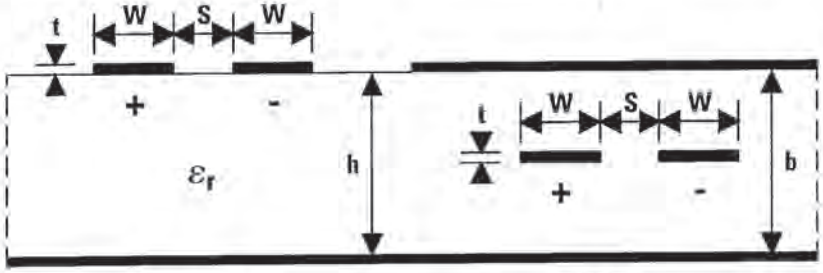
b) Traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance. See section 4.1.3.

c) Edge-coupled Microstrip line offer the advantage that a higher differential Z_O is possible (100 to 150Ω). Also it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

d) Stripline may be either edge-couple or broad-side lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also coupling of noise onto the lines. They also require the use of via to connect to them.

4.1.3 Differential Traces

a) Use controlled impedance PCB traces which match the differential impedance of your transmission medium (i.e. cable) and termination resistor. Route the differential pair traces as close together as possible as soon as they leave the IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.



When designing for a specific differential Z_O (Z_{DIFF}) for edge-coupled lines, it is recommended that you adjust trace width "W" to alter Z_{DIFF}. It is recommended to not adjust "S" which should be the minimum spacing specified by your PCB vendor for line-to-line spacing. You can use National's Transmission Line RAPIDESIGNER slide rule (LIT# 633200-001 metric or LIT# 633201-001 English units) and application note AN-905, LIT# 100905-002) to calculate Z_O and Z_{DIFF}, or you can use the equations below for edge-coupled differential lines:

$$Z_{DIFF} = 2*Z_0 \left(1 - 0.48e^{-0.96\frac{S}{h}}\right) \text{ Ohms} \quad \text{Microstrip}$$

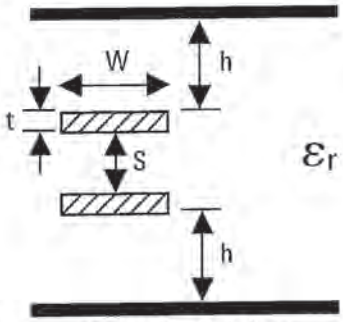
$$Z_{DIFF} = 2*Z_0 \left(1 - 0.374e^{-2.9\frac{S}{h}}\right) \text{ Ohms} \quad \text{Stripline}$$

$$Z_0 = \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8W + t)}\right) \text{ Ohms} \quad \text{Microstrip}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\,\pi\,(0.8W + t)}\right) \text{ Ohms} \quad \text{Stripline}$$

Note: For edge-coupled striplines, the term "0.374" may be replaced with "0.748" for lines which are closely-coupled (S < 12 mils).

Broadside coupled lines structure can also be used. The dimensions for this type of line are shown below. Broadside coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector pin field. An equation with similar accuracy as for the edge-couple lines is:



Broadside Stripline

$$Z_{DIFF} = \frac{80}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(2h+t)}{0.8W+t}\right]\left[1-\frac{h}{4(h+S+t)}\right] \text{ Ohms}$$

Broadside Stripline

Always use consistent dimensions (e.g. all dimensions in mils, centimeters or millimeters) for S, h, W, and t when making calculations.

Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary, please refer to AN-905 for accuracy information and ranges supported.

Common values of dielectric constant (ε_r) for various printed circuit board (PCB) materials is given below. Consult your PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. GETEK is about 1.5 times as expensive as FR-4, but can be considered for 1000+ MHz designs. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

PCB Material	Dielectric Constant (ε_r)	Loss Tangent
Air	1.0	0
PTFE (Teflon)	2.1-2.5	0.0002-0.002
BT Resin	2.9-3.9	0.003-0.012
Polyimide	2.8-3.5	0.004-0.02
Silica (Quartz)	3.8-4.2	0.0006-0.005
Polyimide/Glass	3.8-4.5	0.003-0.01
Epoxy/Glass (FR-4)	4.1-5.3	0.002-0.02
GETEK	3.8-3.9	0.010-0.015 (1MHz)
ROGERS4350 Core	3.48 ± 0.05	0.004 @ 10G, 23°C
ROGERS4430 Prepreg	3.48 ± 0.05	0.005 @ 10G, 23°C

b) Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, $v = c/\varepsilon_r$ where c (the speed of light) = 0.2997mm/ps or 0.0118in/ps). A general rule is to match lengths of the pair to within 100mils.

c) Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to insure isolation between pairs of the differential lines.

d) Minimize the number of via and other discontinuities on the line.

e) Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.

f) Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. Both lines of the pair should be as identical as possible for the best results.

4.1.4 Termination

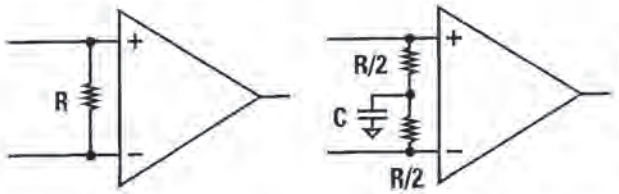
a) Use a termination resistor which best matches the differential impedance of your transmission line. It should be between 90Ω and 130Ω for point-to-point cable applications. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a resistor termination.

b) Typically a single resistor across the pair at the receiver end suffices.

c) Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7mm (12mm MAX).

d) Resistor tolerance of 1 or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match the better. Match to the nominal differential impedance of the interconnect.

d) Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.



Where R = Z_{DIFF} (between 100 and 120Ω), C ≈ 50pF
Components should be surface mount components, placed close to the receiver. Use 1-2% resistors.

Common Differential Termination Schemes

4.1.5 Unused Pins

LVDS INPUTS - Leave unused LVDS receiver inputs open (floating) for LVDS receiver unless directed differently by the specific component's datasheet. Their internal failsafe feature will lock the outputs high. These unused receiver inputs should not be connected to noise sources like cables or long PCB traces — float them near the pin. LVDS receivers are high-speed, high-gain devices, and only a small amount of noise, if picked up differentially will cause the receiver to respond. This causes false transitions on the output and increased power consumption.

LVDS & TTL OUTPUTS - Leave all unused LVDS and TTL outputs open (floating) to conserve power. Do not tie them to ground.

TTL INPUTS - Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground or in certain cases they may be left open if the datasheet supports this condition. Some devices provide internal pull down (or up) devices to bias the pins. Again, consult the datasheet for information regarding the device's features. This type of information is typically included in the pin description table.

4.1.6 Probing LVDS Transmission Lines

a) Always use a high impedance (>100kΩ), low capacitance (<0.5pF) probe/scope with a wide bandwidth (>1GHz). Improper probing will give deceiving results. LVDS is not intended to be loaded with a 50Ω load to ground. This will distort the differential and offset voltages of the driver. Differential probes are recommended over two standard scope probes due to match and balance concerns. Bandwidth of the probe/scope combination should be at least 1 or 2GHz. Tektronix and Agilent (HP) both make probes that are well suited for measuring LVDS signals. (See Chapter 7)

4.1.7 Loading LVDS I/O – Preserving Balance

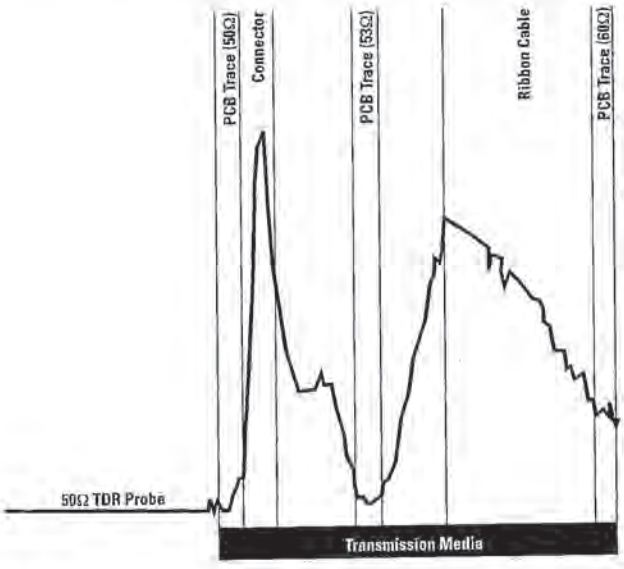
Avoid placing any devices which heavily load the low, ~3.5mA LVDS output drive. If additional ESD protection devices are desired, use components which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

Try not to disturb the differential balance. Treat both members of a pair equally.

4.2.0 RESULTS OF GOOD VS. BAD DESIGN PRACTICES

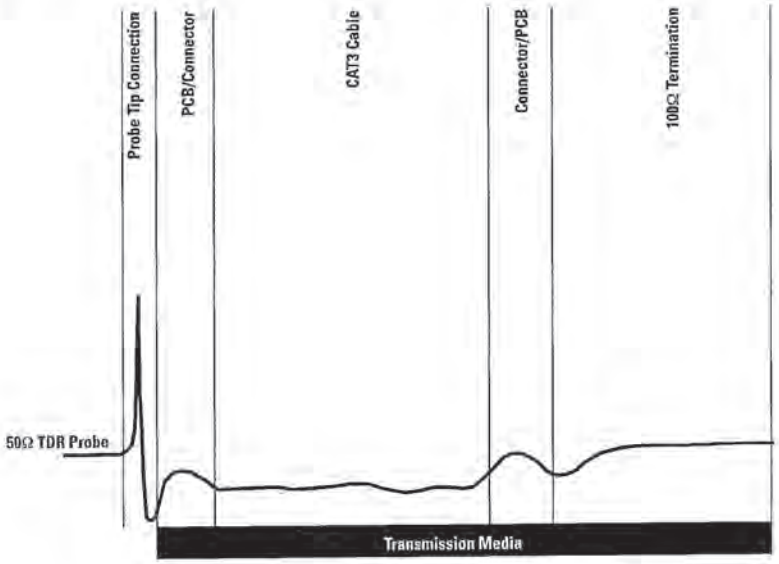
4.2.1 Impedance Mismatches

It is very common for designers to automatically use any off-the-shelf cables and connectors and 50Ω autorouting when doing new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low swing, current-mode outputs to reduce noise, but that its transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable are not meant for high-speed signals (especially differential signals) and do not always have controlled impedance. The figure below shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedances are neither matched nor controlled. Beware, this example is not worst case — it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.



TDR plot of transmission media with mismatched impedance.

Below is a much improved design which follows most of the high-speed differential design practices listed in Section 4.1.0. The TDR differential impedance plot is much flatter and noise is dramatically reduced.

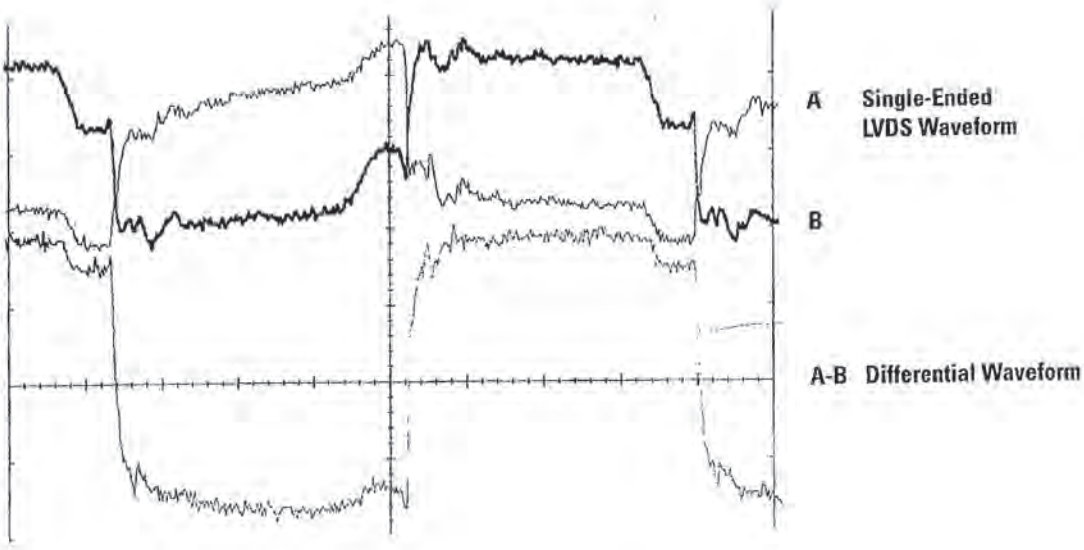


Minimize impedance variations for best performance.

4.2.2 Crosstalk Between TTL and LVDS Signals

The next two figures show the effects of TTL coupling onto LVDS lines. The first figure shows the LVDS waveforms before coupling, while the second shows the effects of a 25MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 inches. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally — the signal which runs closest to the TTL trace is affected more than the other. This difference will not be rejected by the receiver as common-mode noise and though it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal reducing noise margin. The common-mode noise will be rejected by the receiver, but can radiate as EMI.

LVDS Signals Before Crosstalk



LVDS signals affected by TTL crosstalk.

4.2.3 The "S" Rule

Using the edge-to-edge "S" distance between the traces of a pair, other separations can be defined:

- The distance between two pairs should be >2S.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.

4.3.0 LOWERING ELECTROMAGNETIC INTERFERENCE (EMI)

4.3.1 LVDS and Lower EMI

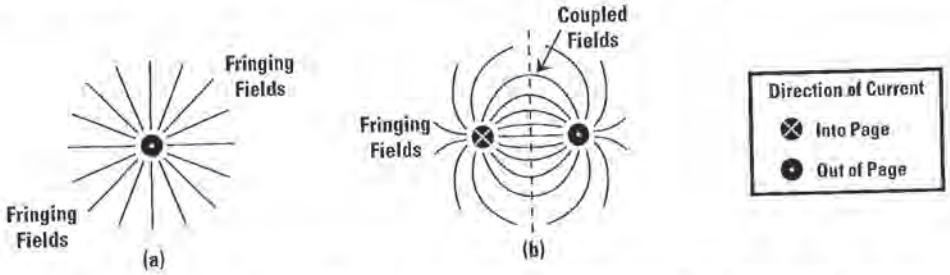
High-speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1. The low output voltage swing (~350mV)
2. Relatively slow edge rates, dV/dt ~ 0.350V/0.350ns = 1V/ns
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. "Soft" output corner transitions
5. Minimum I_{CC} spikes due to low current-mode operation and internal circuit design

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

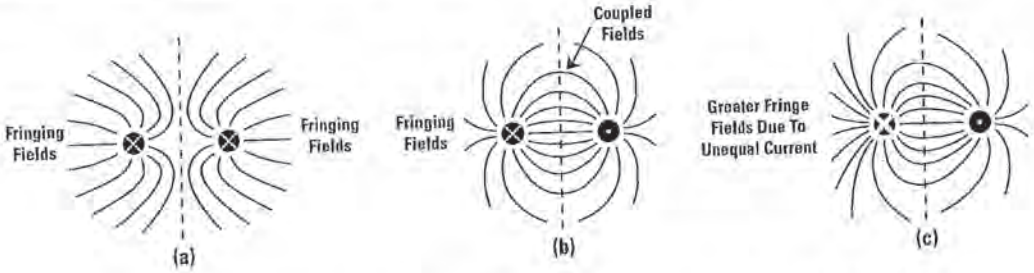
4.3.2 Electromagnetic Radiation of Differential Signals

Today's increasing data rates and tougher electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves which can escape through shielding causing a system to fail EMC tests. Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another). In single-ended lines like CMOS/TTL shown below, almost all the electric field lines are free to radiate away from the conductor. These fields may be intercepted by other objects, but some can travel as TEM waves which may escape the system causing EMI problems.



Electromagnetic field cancellation in differential signals (b) through coupling versus a single-ended signal (a).

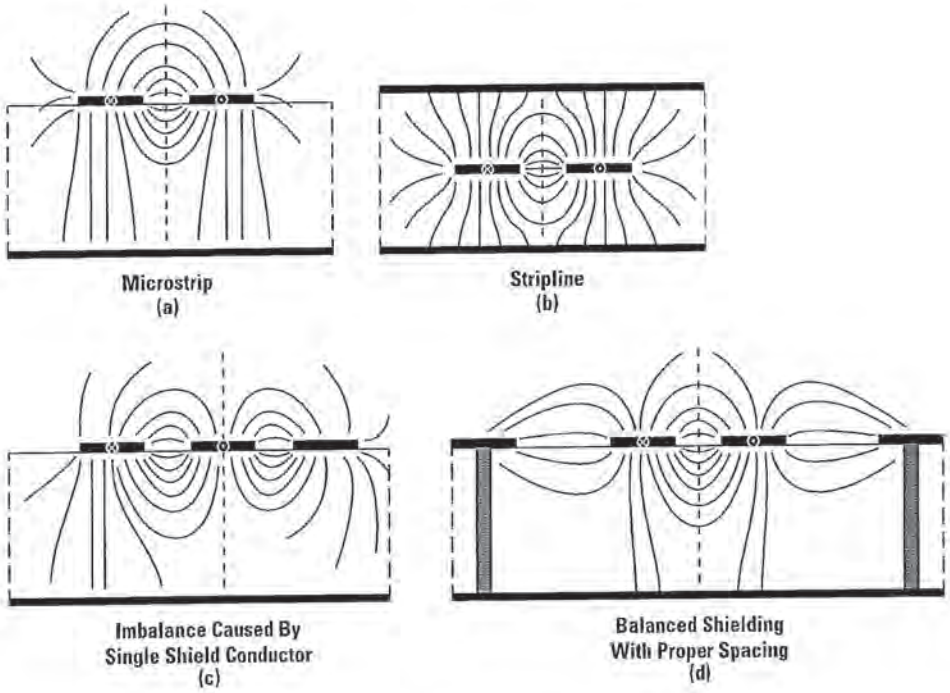
Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic fields lines tend to cancel and the electric fields (shown above) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals much less field energy is available to propagate as TEM waves versus single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.



Even or common-mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines.

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in (a) above, but factors can cause an imbalance in currents (c) versus the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown below. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field.lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_O (Z_{DIFF}). More shielding can be achieved using microstrip without significantly impacting propagation velocity using shield traces as in (d), but be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace — or any trace — on one side (c) creates an imbalance which can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<1/4 wavelength) intervals, and should be placed at least 2S from the pair.

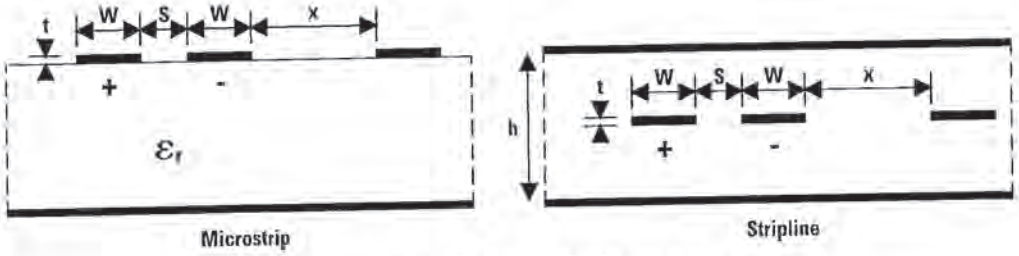


Ideal differential signals on microstrip a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d).

4.3.3 Design Practices for Low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are close coupling between the conductors of each pair and minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown next. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors to preserve closer coupling between the conductors versus the power and ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

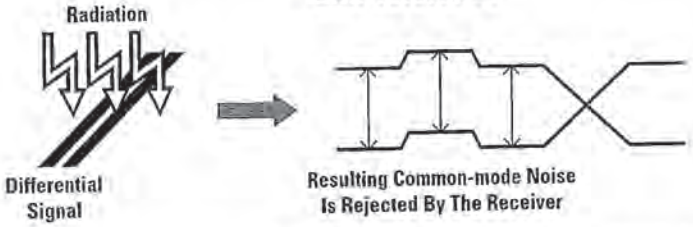


For good coupling, make S < 2W, S < h, and x ≥ 2W & 2S.

For sufficient coupling (canceling) of electromagnetic fields, the distance between the "+" and "–" signal should be minimized.

Close coupling between conductors of a pair not only reduces EMI, but it helps to ensure noise coupled onto the conductors will do so equally as common-mode noise which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.

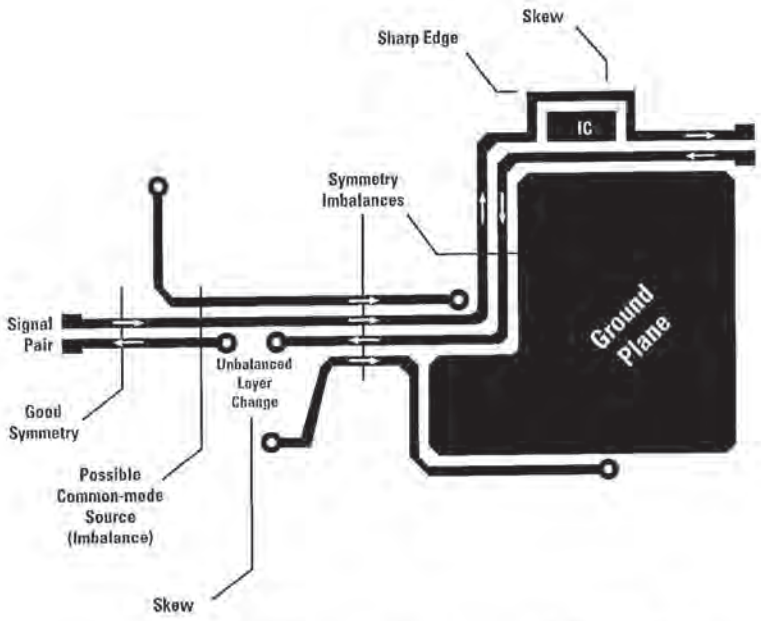
EMI Tolerance



Close coupling not only reduces EMI, but improves EMI tolerance too.

Imbalance minimization is the other important factor in reducing EMI. Although fields result from the complex interaction between objects of a system and are difficult to predict (especially in the dynamic case), certain generalizations can be made. The impedance of your signal traces should be well-controlled. If the impedance of one trace changes versus another, the voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

The basic rule to follow is: if any discontinuity must be introduced in proximity to differential lines, it should introduced equally to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, PCB traces, etc. Remember that the key word is balance.



This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation.

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Since fields are proportional to voltage/current amplitude at any given point in time, any factors affecting the time (delay, velocity, etc.) and/or amplitude (attenuation, etc.) properties of the signals can increase EMI and can be seen on a scope. The next figure illustrates how waveforms — easily seen on a scope — can help predict far field EMI. First, the beneficial field canceling effects of ideal differential signals (b) versus single-ended signals (a) are compared.

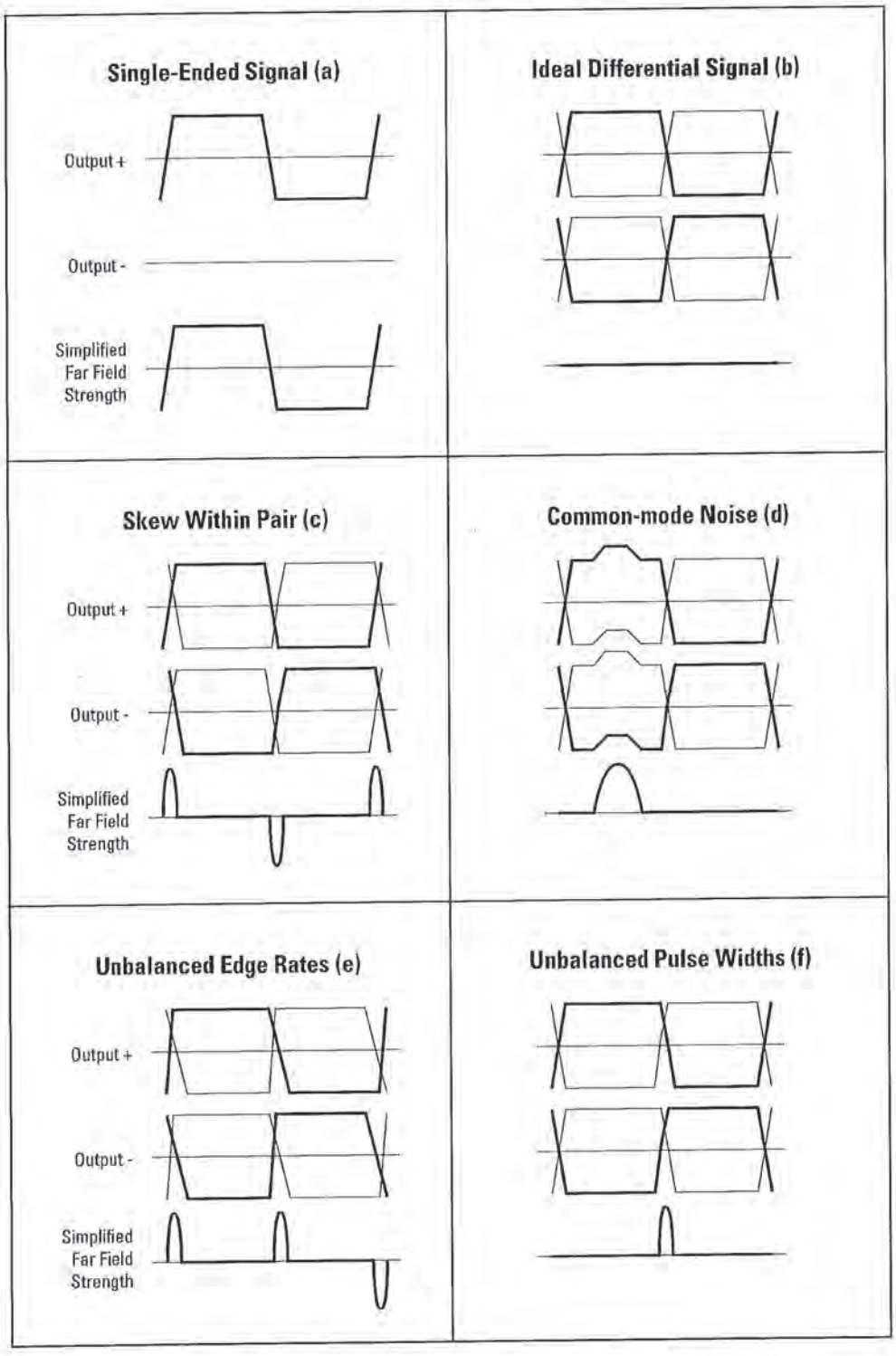
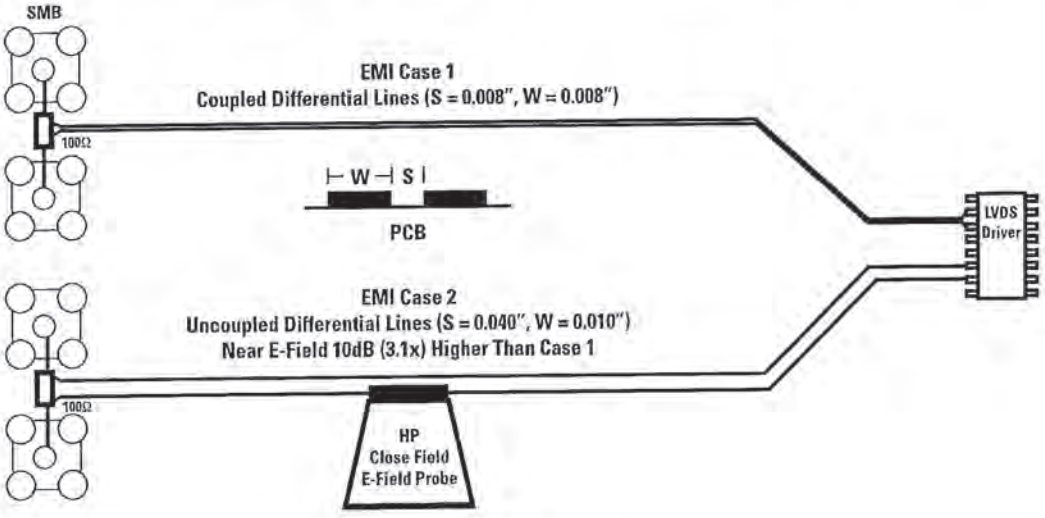


Diagram showing simplified far field radiation under various situations.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common-mode noise, unbalanced attenuation, etc. These affect the relative amplitudes of the fields at any given moment, reducing the canceling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

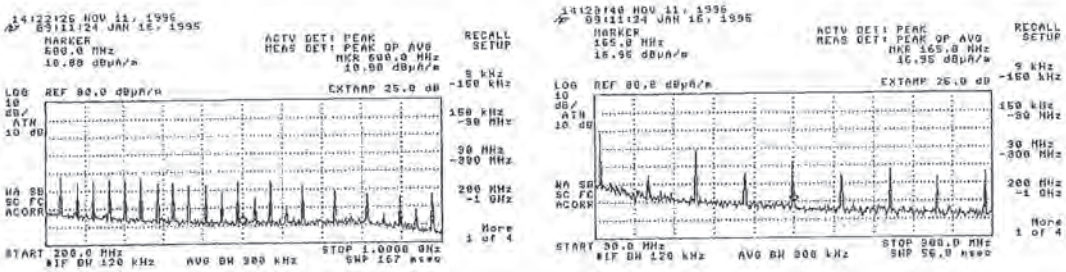
4.3.4 EMI Test Results

The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals versus uncoupled signals. The setup compares two sets of LVDS signals: one set in which pair spacing is less than trace width (S < W) and another set in which S >> W so that the pair members are no longer closely coupled (though the differential impedance of the transmission line is still 100Ω).



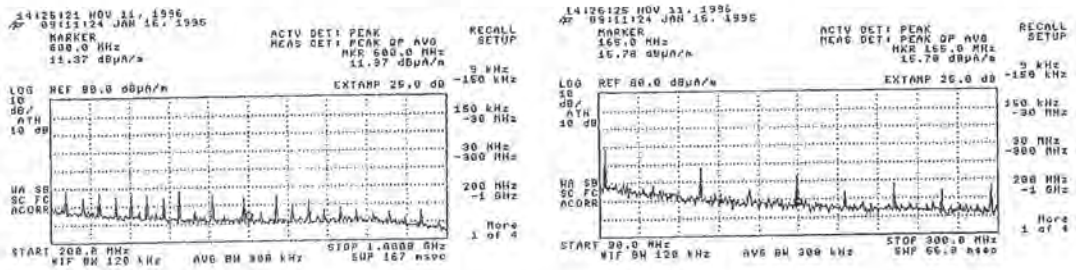
EMI Test Setup

Near (close) field electric field measurements were made for both cases while using a 32.5MHz 50% duty cycle clock as the source. The two plots below show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200MHz to 1GHz. The second plot looks more closely at the frequencies between 30MHz and 300MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.



Near E-Field Strength for Uncoupled Signals
(Case 2): 200MHz-1GHz *(Case 2): 30MHz-300MHz*

The next two plots show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.



Near E-Field Strength for Closely Coupled Signals

(Case 1): 200MHz-1GHz *(Case 1): 30MHz-300MHz*

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The closely coupled pair showed about 10dB (>3 times) lower electric field strength than the uncoupled pair.

This test illustrates two things:

1. Use of differential signals versus single-ended signals can be used effectively to reduce emissions.
2. The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than is seen here.

4.3.5 Ground Return Paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance.

Since LVDS is differential, the signal current that flows in one conductor of a pair will flow back through the other conductor, completing the current loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common-mode noise current which must return also. This common-mode current will be capacitively coupled to ground and return to the driver through the path of least impedance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems.

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common-mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least impedance and means that the current loop area is minimized.

Similarly, in cables, a ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area. (See Chapter 5 on Cables).

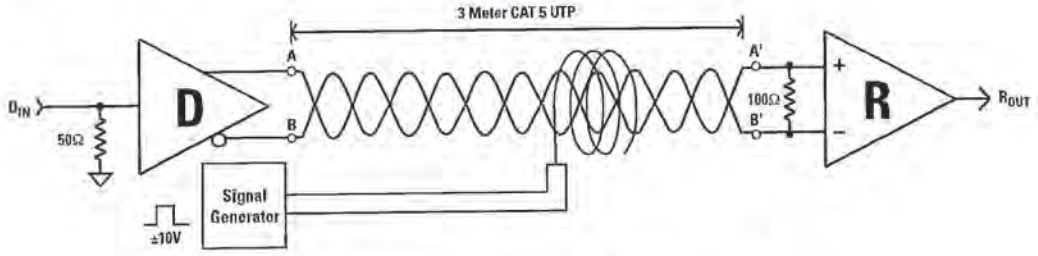
4.3.6 Cable Shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (see Chapter 5).

4.3.7 EMC Conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled and matched.

4.4.0 COMMON-MODE NOISE REJECTION



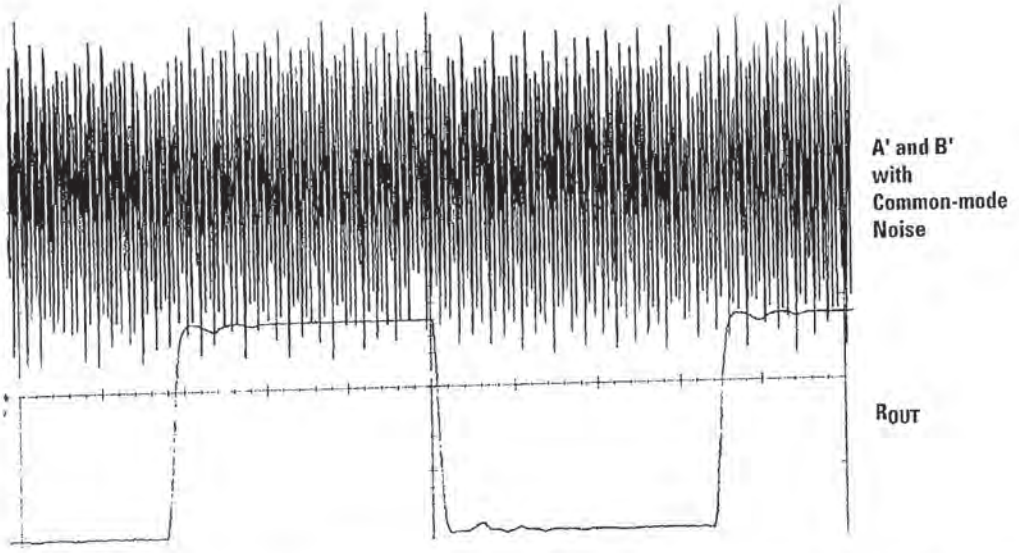
Common-mode noise rejection test setup.

Test Setup:

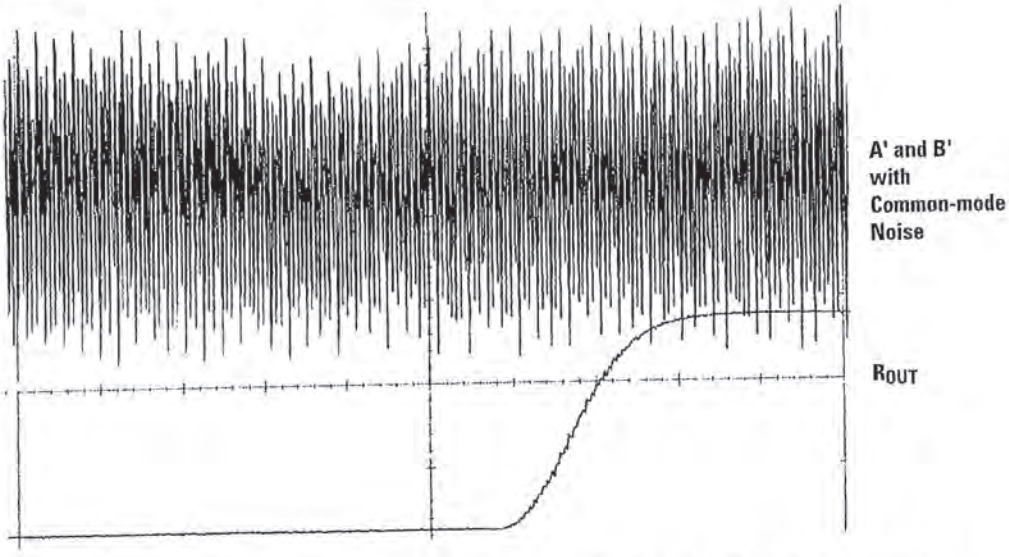
Driver: DS90C031 (one channel)
Receiver: DS90C032 (one channel)
V_{CC} = 5V
T_a = 25°C

This test demonstrates the common-mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (±350mV swing with <±100mV thresholds). Provided that the differential signals run close together through controlled impedance media, however, most of the noise on LVDS lines will be common-mode. In other words, EMI, crosstalk, power/ground shifts, etc. will appear equally on each pair and this common-mode noise will be rejected by the receiver. The plots below show common-mode noise rejection with V_{CM} noise up to −0.5V to +3.25V peak-to-peak.

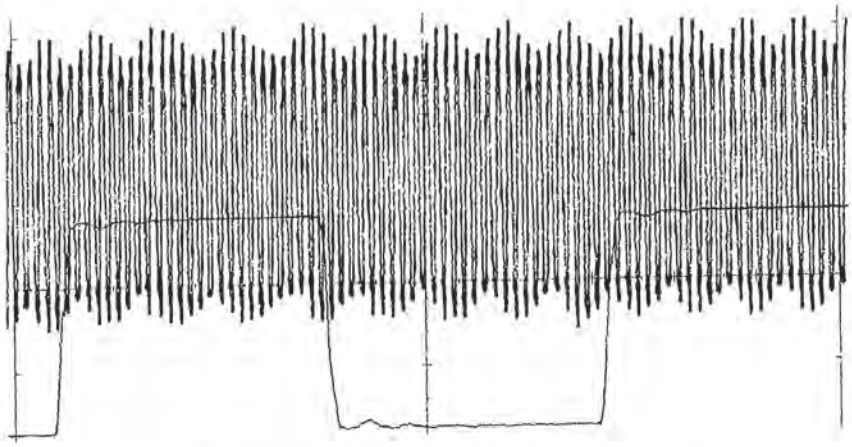
Reference waveform showing LVDS signal and receiver output.



Coupled common-mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output.



Expanded view of coupled common-mode noise waveform and clean receiver output.



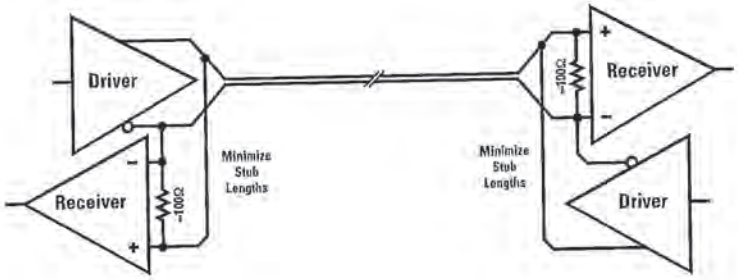
Clean receiver output despite –0.5V to +3.25V peak-to-peak common-mode noise.

4.5.0 LVDS CONFIGURATIONS

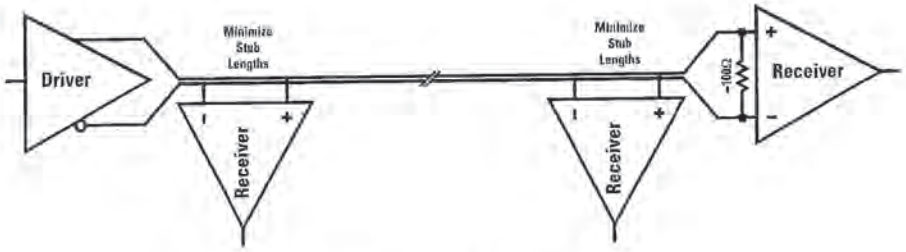
Point-to-point configuration.

Although LVDS drivers and receivers are typically used in a point-to-point arrangement (above), other topologies are possible. The point-to-point configuration does provide the best signal path and should be used for very high-speed interconnect links. Point-to-point links are commonly used in conjunction with crosspoint switches.

The configuration shown below allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin) if using standard LVDS drivers. A better solution would be to employ Bus LVDS (BLVDS) drivers which are designed for double termination loads. They provide levels compatible with LVDS and do not trade off noise margin. Common-mode range for LVDS and BLVDS is ±1V (typical), so cable lengths tend to be in the tens of meters.

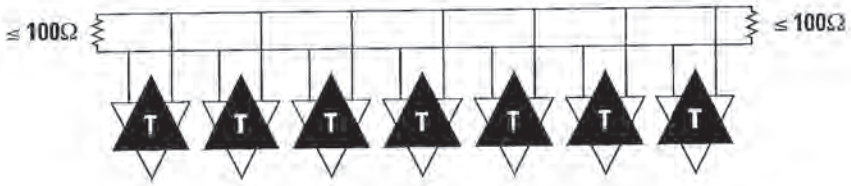


Bi-directional half-duplex configuration.



Multidrop configuration.

Since LVDS receivers have high impedance inputs, a multidrop configuration can also be used if transmission distance is short and stub lengths are less than ~12mm (as short as possible). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down. This application is good when the same set of data needs to be distributed to multiple locations.



Multipoint Configuration.

A multipoint bus supports multiple drivers, but only one is allowed to be active at any given time. With Bus LVDS devices, double terminated busses can be used without trading off signal swing and noise margin. Termination should be located at both ends of the bus. Failsafe biasing should be considered if a known state on the bus is required when all drivers are in TRI-STATE®. As with the multidrop bus, stubs off the mainline should be kept as short as possible to minimize transmission line problems.

4.6.0 FAILSAFE BIASING OF LVDS

4.6.1 Most Applications

Most LVDS receivers have internal failsafe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Always consult the component's datasheet to determine which type of failsafe protection is supported. Here is a summary of LVDS failsafe conditions:

OPEN INPUT PINS - Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state. This minimizes power dissipation and switching noise.

TERMINATED INPUT PINS - If the cable is removed and the inputs to the receiver have a termination resistor across them, then the output will be stable (HIGH). Noise picked up at the input, if differential in nature, can cause the device to respond. If this is the case see section 4.6.2 below.

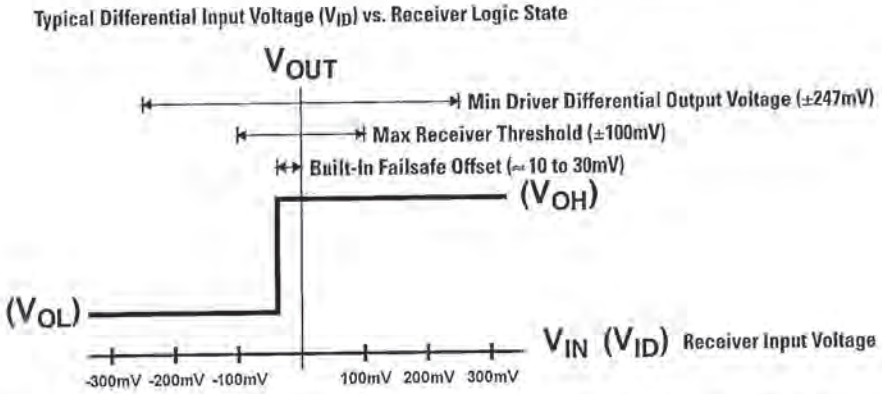
TERMINATED INPUT PINS - Noisy Environments - See section 4.6.2 if failsafe must be guaranteed in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE®.

SHORTED INPUTS - The receiver output will remain in a high state when the inputs are shorted. This is considered a fault condition protection only. It is not specified across the input voltage range of the receiver.

4.6.2 Boosting Failsafe In Noisy Environments

The internal failsafe circuitry is designed to source/sink a very small amount of current, providing failsafe protection for floating receiver inputs, shorted receiver inputs, and terminated receiver inputs as described above and in the component's datasheet. It is not designed to provide failsafe in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE®. When this happens, the cable becomes a floating antenna which can pick up noise. If the cable picks up more differential noise than the internal failsafe circuitry can overcome, the receiver may switch or oscillate. If this condition can happen in your application, it is recommended that you choose a balanced and/or shielded cable which will reduce the amount of differential noise on the cable. In addition, you may wish to add external failsafe resistors to create a larger noise margin. However, adding more failsafe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore, a compromise should be the ultimate goal.

4.6.3 Choosing External Failsafe Resistors



External failsafe can be added, but must be small enough not to significantly affect driver current.

The chart above shows that National's present LVDS devices typically have an internal failsafe voltage of about -10 to -30mV. If the receiver will not always be driven by the driver in your application and the cable is expected to pick up more than 10mV of differential noise you may need to add additional failsafe resistors. The resistors are chosen by first measuring/predicting the amount of differential-mode noise you will need to overcome. V_{FSB} is the offset voltage generated across the termination resistor (100Ω). Note that you do not need to provide a bias (V_{FSB}) which is greater than the receiver threshold (100mV), typically +15mV or +20mV is sufficient. You only need enough to overcome the differential noise, since the internal failsafe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

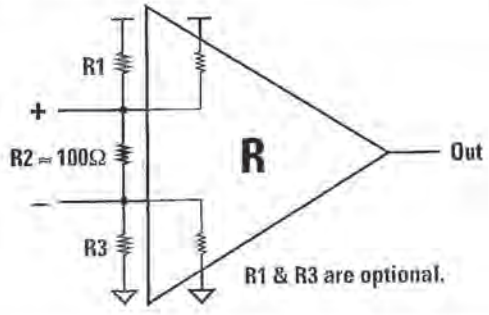


Diagram showing simplified internal failsafe circuitry and optional external "helper" failsafe resistors.

For best results, follow these procedures when choosing external failsafe resistors:

1. First ask the question "Do I need external failsafe?" If your LVDS driver is always active, you will not need external failsafe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential-mode noise, you may not need to boost failsafe.

2. Measure/predict the amount of differential-mode noise at the receiver end of the cable in worst case conditions. If you have a lot of noise, use a balanced cable like twisted pair which tends to pick up mostly common-mode noise, not differential-mode noise. Do not use simple ribbon cables which can pick up differential-mode noise due to fixed positions of the conductors.

   Use a shielded cable if possible. Using a balanced and/or shielded cable is best way to prevent noise problems in noisy environments.

3. Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst case conditions. Set this equal to V_{FSB} in the equation below and solve for the external failsafe resistors R1 and R3.

$$V_{FSB} = \frac{R2}{R1 + R2 + R3} V_{CC}$$

$$I_{BIAS} = \frac{V_{CC}}{R1 + R2 + R3} << I_{LOOP} \quad (\text{Use } I_{BIAS} \leq 0.1 * I_{LOOP})$$

$$V_{CM} = \frac{R3 + R2/2}{R1 + R2 + R3} V_{CC} = 1.2V \Rightarrow R1 \approx R3 \left(\frac{V_{CC}}{1.2V} - 1 \right)$$

$$R_{TEQ} = \frac{R2\,(R1 + R3)}{R1 + R2 + R3} = \text{match transmission line } Z_{ODIFF}$$

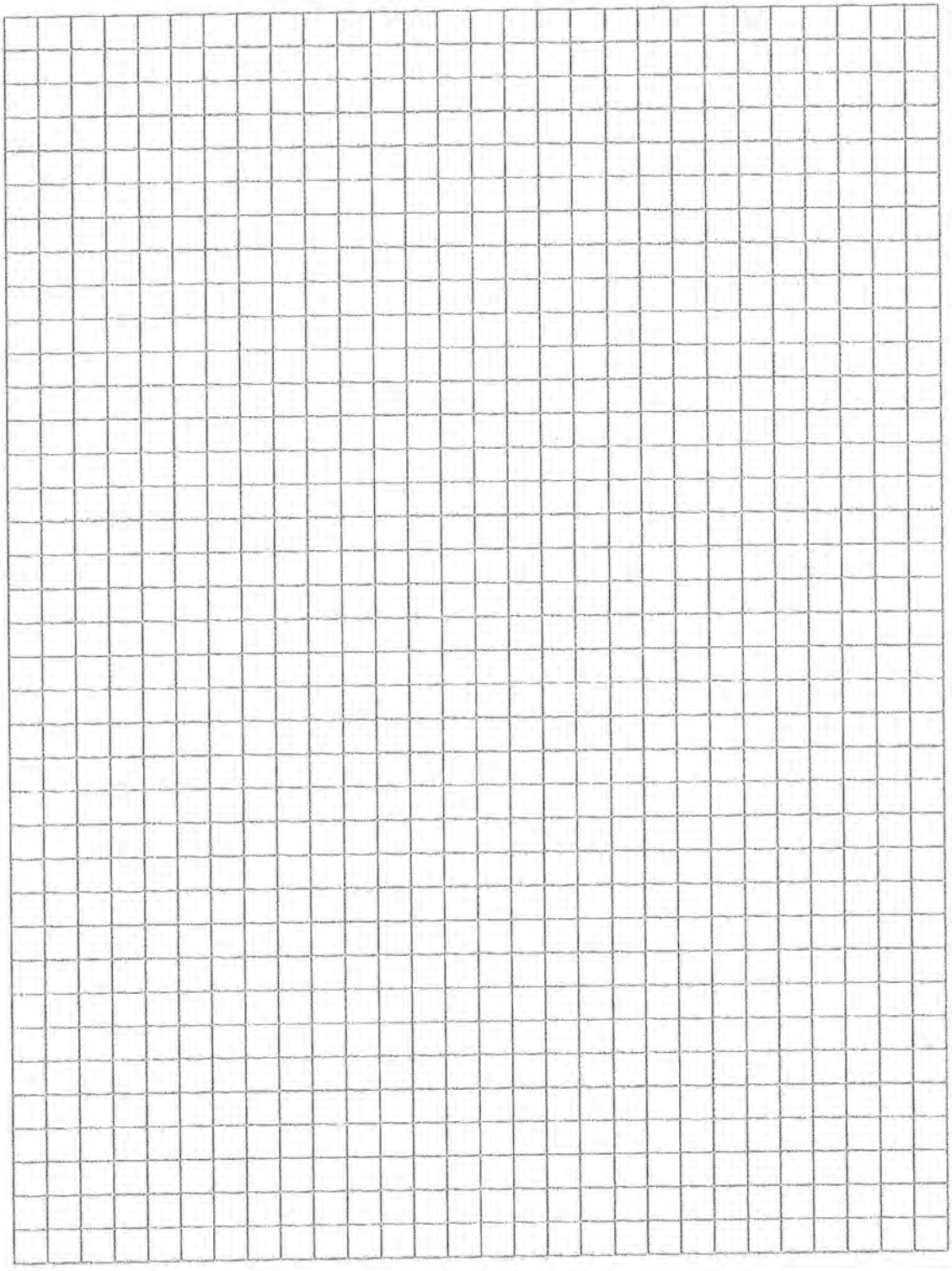
4. You now have an equation relating R1 to R3. Choose R1 and R2 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R2 should be greater than 20kΩ for V_{CC} = 5V and greater than 12kΩ for V_{CC} = 3.3V. Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.

5. The external failsafe resistors may change your equivalent termination resistance, R_{TEQ}. Fine tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

4.7.0 POWER-OFF HIGH IMPEDANCE BUS PINS

Power off high impedance is a useful feature, most 2nd and 3rd generation LVDS receivers provide this feature. This is typically listed as a feature and also as a condition of the I_{IN} parameter. This feature is useful in applications that employ more than one receiver and they are powered from local power supplies. If the power is turned off to one node, it should not load down the line and prevent communication between other powered-up nodes.

NOTES



Cables, Connectors and Performance Testing

Chapter 5

5.0.0 CABLES, CONNECTORS AND PERFORMANCE TESTING

5.1.0 GENERAL COMMENTS

When choosing cables and connectors for LVDS it is important to remember:

1. Use controlled impedance media. The cables and connectors you use should have a differential impedance of about 100Ω. They should not introduce major impedance discontinuities that cause signal reflections.

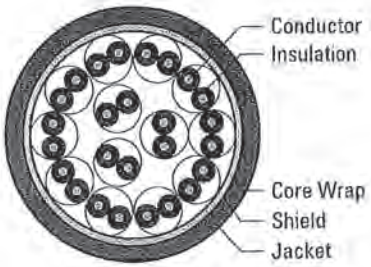
2. Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.

3. For cable distances < 0.5m, most cables can be made to work effectively. For distances 0.5m < d < 10m, CAT 3 (Category 3) twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

5.2.0 CABLING SUGGESTIONS

As described above, try to use balanced cables (twisted pair, twin-ax, or flex circuit with closely coupled differential traces). LVDS was intended to be used on a wide variety of media. The exact media is not specified in the LVDS Standard, as it is intended to be specified in the referencing standard that specifies the complete interface. This includes the media, data rate, length, connector, function, and pin assignments. In some applications that are very short (< 0.3m), ribbon cable or flex circuit may be acceptable. In box-to-box applications, a twisted pair or twin-ax cable would be a better option due to robustness, shielding and balance. Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

5.2.1 Twisted Pair



Drawing of Twisted Pair Cable, Cross-Section

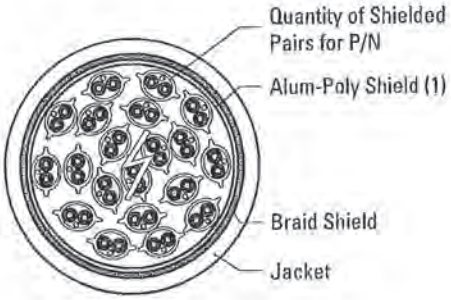
Twisted pair cables provide a good, low cost solution with good balance, are flexible, and capable of medium to long runs depending upon the application skew budget. It is offered with an overall shield or with shields around each pair as well as an overall shield. Installing connectors is more difficult due to its construction.

a) Twisted pair is a good choice for LVDS. Category 3 (CAT3) cable is good for runs up to about 10m, while CAT5 has been used for longer runs.

b) For the lowest skew, group skew-dependent pairs together (in the same ring to minimize skew between pairs).

c) Ground and/or terminate unused conductors (do not float).

5.2.2 Twin-ax Cables



Drawing of Individually Shielded Parallel Pair Twin-ax Cable - Cross Section

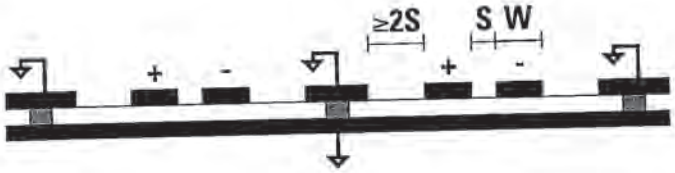
Twin-ax cables are flexible, have low skew and shields around each pair for isolation. Since they are not twisted, they tend to have very low skew within a pair and between pairs. These cables are for long runs and have been commonly deployed in Channel Link and FPD-Link applications.

a) Drain wires per pair may be connected together in the connector header to reduce pin count.

b) Ground and/or terminate unused conductors.

5.2.3 Flex Circuit

Flex circuit is a good choice for very short runs, but it is difficult to shield. It can be used as an interconnect between boards within a system.



Flex Circuit - Cross-Section

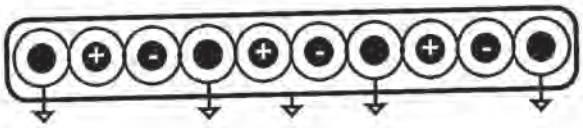
a) Closely couple the members of differential pairs (S < W). Do not run signal pairs near the edges of the cable, as these are not balanced.

b) Use a ground plane to establish the impedance.

c) Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

5.2.4 Ribbon Cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well suited for high-speed differential signaling (good coupling is difficult to achieve), but it is OK for very short runs.



Flat Cable - Cross-Section

a) If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.

b) Use shielded cable if possible, shielded flat cable is available.

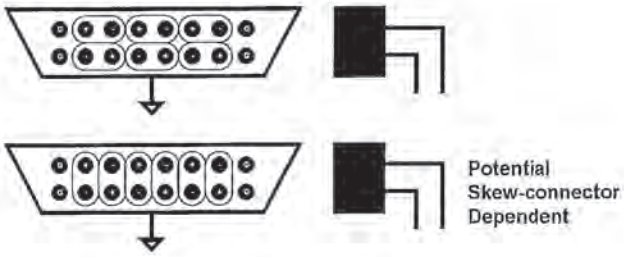
5.2.5 Additional Cable Information

Additional information on cable construction may be found in National Application Note AN-916. Also, many cable, connector and interconnect system companies provide detailed information on their respective websites about different cable options. A non-inclusive list of a few different options is provided below:

3M	www.3M.com/interconnects/
Spectra-Strip Cable Products	www.spectra-strip.amphenol.com/default.CFM
AMP	http://connect.amp.com/

5.2.6 Connectors

Connectors are also application dependent and depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Standard connectors have been used at low to medium data rates, and optimized low skew connectors have been developed for medium to high-speed applications.



Typical Connector Pinouts

a) Choose low skew, impedance matching connectors if possible.

b) Group members of each pair together. Pins of a pair should be close together (adjacent) not separated from each other. This is done to maintain balance, and to help ensure that external noise, if picked up, will be common-mode and not differential in nature.

c) Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins that yield the lowest skew and crosstalk for your particular connector. Shorter pin lengths tend to be better than long ones, minimize this distance if possible.

d) Place ground pins between pairs where possible and convenient. Especially use ground pins to separate TTL/CMOS signals for LVDS signals.

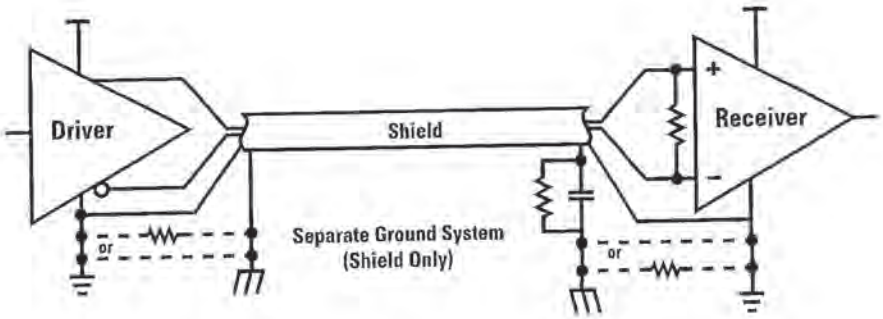
e) Ground end pins. Do not use end pins for high-speed signals, if possible, as they offer less balance.

f) Ground and/or terminate unused pins.

Many different connector options exist. One such cable-connector system that has been used for LVDS with great results is the 3M "High-speed MDR Digital Data Transmission System." This cable system is featured on the National Channel-Link (48-bit) and LDI Evaluation Kits. The connector is offered in a surface mount option that has very small skew between all the pins. Different cable types are also supported.

5.3.0 CABLE GROUND AND SHIELD CONNECTIONS

In many systems, cable shielding is required for EMC compliance. Although LVDS provides benefits of low EMI when used properly, shielding is still usually a good idea especially for box-to-box applications. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the pair shield or drain wire in some cables) and provides a small loop area return path for common-mode currents. Typically one or more pairs are assigned to ground (circuit common). Using one or more pair reduces the DCR (DC Resistance) of the path by the parallel connection of the conductors. This provides a known, very low impedance return path for common-mode currents.



Typical Grounding Scheme

In most applications the grounding system will be common to both the receiver and the driver. The cable shield is connected at one end with a DC connection to the common ground (frame ground). Avoid "pig-tail" (high inductance) ground wiring from the cable. The other end of the shield is typically connected with a capacitor or network of a capacitor and a resistor as shown in the above example. This prevents DC current flow in the shield. In the case where connectors are involved that penetrate the system's enclosure, the cable shield must have a circumferential contact to the connector's conductive backshell to provide an effective shield and must make good contact.

Note: It is beyond the scope of this book to effectively deal with cabling and grounding systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding and grounding.

5.4.0 LVDS SIGNAL QUALITY

Signal quality may be measured by a variety of means. Common methods are:

- Measuring rise time at the load
- Measuring Jitter in an Eye Pattern
- Bit Error Rate Testing
- Other means

Eye Patterns and Bit Error Rate Testing (BERT) are commonly used to determine signal quality. These two methods are described next.

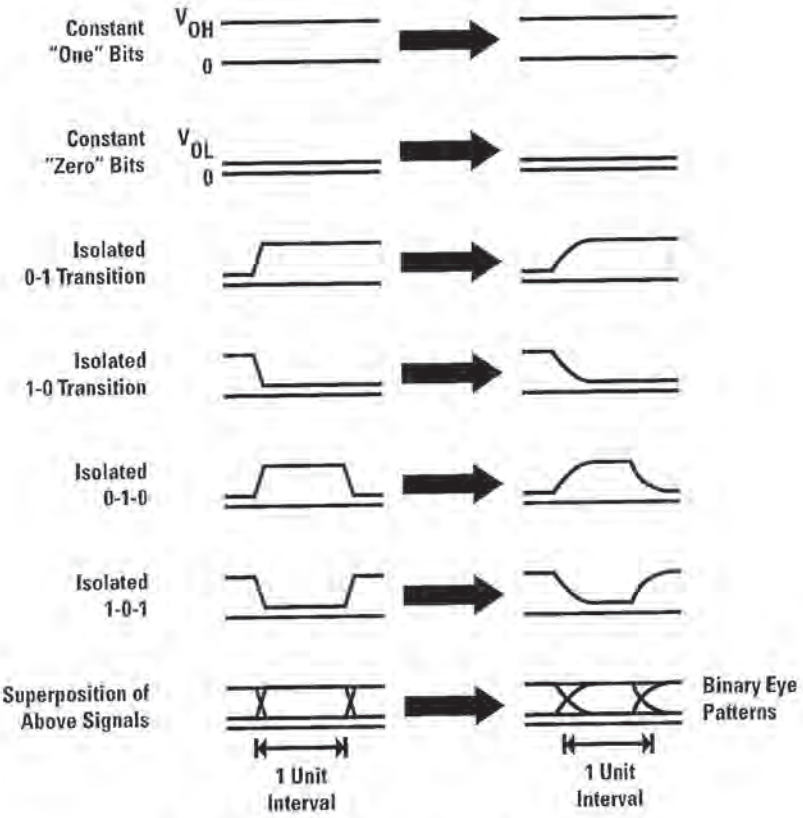
5.4.1 LVDS Signal Quality: Jitter Measurements Using Eye Patterns

This report provides an example of a data rate versus cable length curve for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and the printed circuit boards (PCB). Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment — or even better — in the actual application. Eye pattern measurements are useful in measuring the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

5.4.2 Why Eye Patterns?

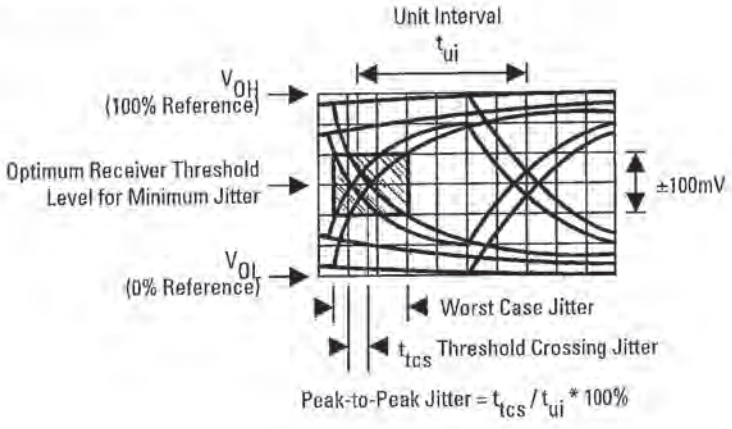
The eye pattern is used to measure the effects of inter-symbol interference on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for NRZ data that does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects of the cable. The next figure illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller (see application note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter-symbol distortion as is a data line.



Formation of an Eye Pattern by Superposition.

The figure below describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between −100mV and +100mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100mV and the jitter measured between the first and last crossing at ±100mV. If the vertical axis units in the figure were 100mV/division, the worse case jitter is at ±100mV levels.



NRZ Data Eye Pattern.

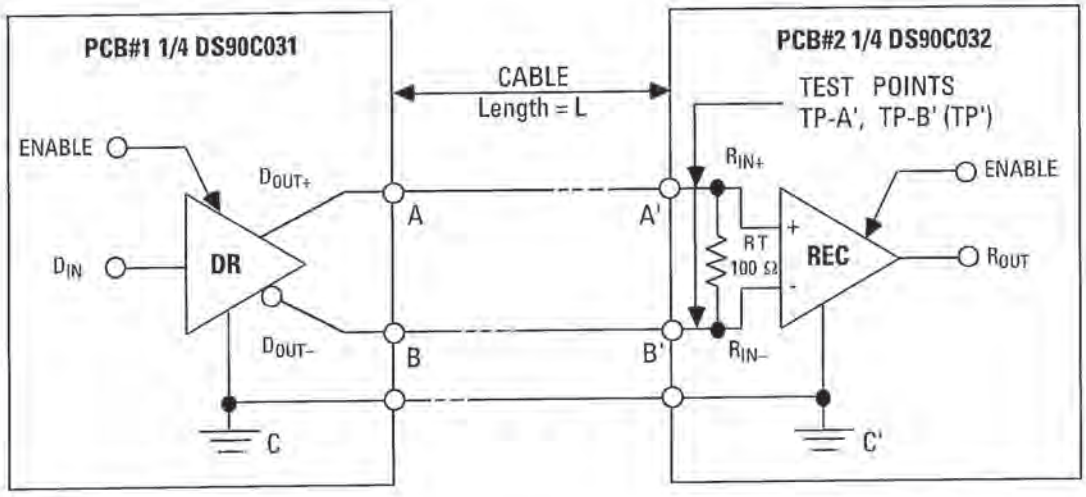
5.4.3 Eye Pattern Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the figure below. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: The cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report, the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer that 10 meters were not tested, but may be employed at lower data rates.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS Signal Quality Test Circuit

5.4.4 Test Procedure

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. Jitter was first measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone and although this will result in a much lower jitter point, it ignores the fact that the receivers may not switch at that very point. For this reason, this signal quality test report measured jitter at both points.

5.4.5 Results and Data Points

20% Jitter Table @ 0V Differential (Minimum Jitter)

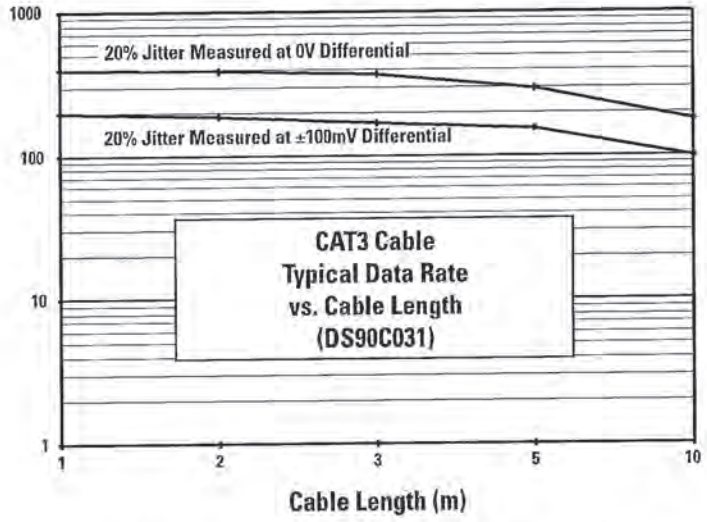
Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the 0V differential point. For the case with the 1 meter cable, 490ps of jitter at 400Mbps was measured, and with the 10 meter cable, 1.160ns of jitter at 180Mbps was measured.

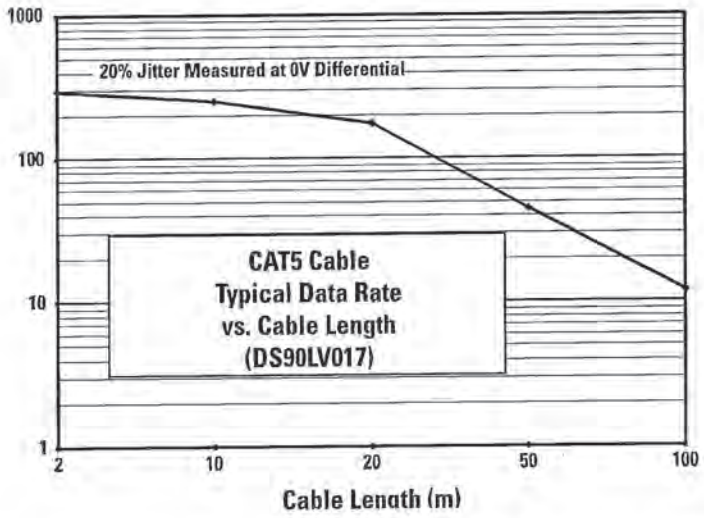
20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (m)	Data Rate (Mbps)	Unit Interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100mV levels. For the 1 meter cable, 1ns of jitter was measured at 200Mbps, and for the 10 meter cable, 2ns of jitter occurred at 100Mbps.



Typical Data Rate vs Cable Length for 0-10m CAT3 Cable



Typical Data Rate vs Cable Length for 2-100m CAT5 Cable (See AN-1088)

Care should be taken in long cable applications using LVDS. When directly coupled, LVDS provides up to ±1V common-mode rejection. Long cable applications may require larger common-mode support. If this is the case, transformer coupling or alternate technologies (such as RS-485) should be considered.

The figures above are a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200-400 Mbps are possible at shorter lengths, and rates of 100-200Mbps are possible at 10 meters. Note that employing a different coding scheme, cable, wire gauge (AWG), etc. will create a different relationship between maximum data rate versus cable length. Designers are greatly encouraged to experiment on their own.

5.4.6 Additional Data on Jitter & Eye Patterns

For additional information on LVDS "Data Rate vs Cable Length" please consult the list of LVDS application notes on the LVDS web site at: **www.national.com/appinfo/lvds/**

At this time of this printing the following application notes were available:

AN#	Devices Tested
AN-977	DS90C031/032
AN-1088	DS90LV017/027, DS92LV010A

5.4.7 Conclusions – Eye Pattern Testing

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate versus distance for a common, inexpensive type of cable.

5.5.0 BIT ERROR RATE (BER) TESTING

Bit error rate testing is another approach to determine signal quality. This test method is described next.

5.5.1 LVDS Cable Driving Performance using BERT

The questions of: "How Far?" and "How Fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example — see application note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector and information about the printed circuit boards (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/032 LVDS Quad Line driver/receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

5.5.2 What is a BER Test?

Bit Error Rate testing is one way to measure of the performance of a communications system. The standard equation for a bit error rate measurement is:

Bit Error Rate = (Number of Bit errors)/(Total Number of Bits)

Common measurement points are bit error rates of:

$\leq 1 \times 10^{-12}$ => One or less errors in 1 trillion bits sent

$\leq 1 \times 10^{-14}$ => One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50Mbps, and the benchmark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

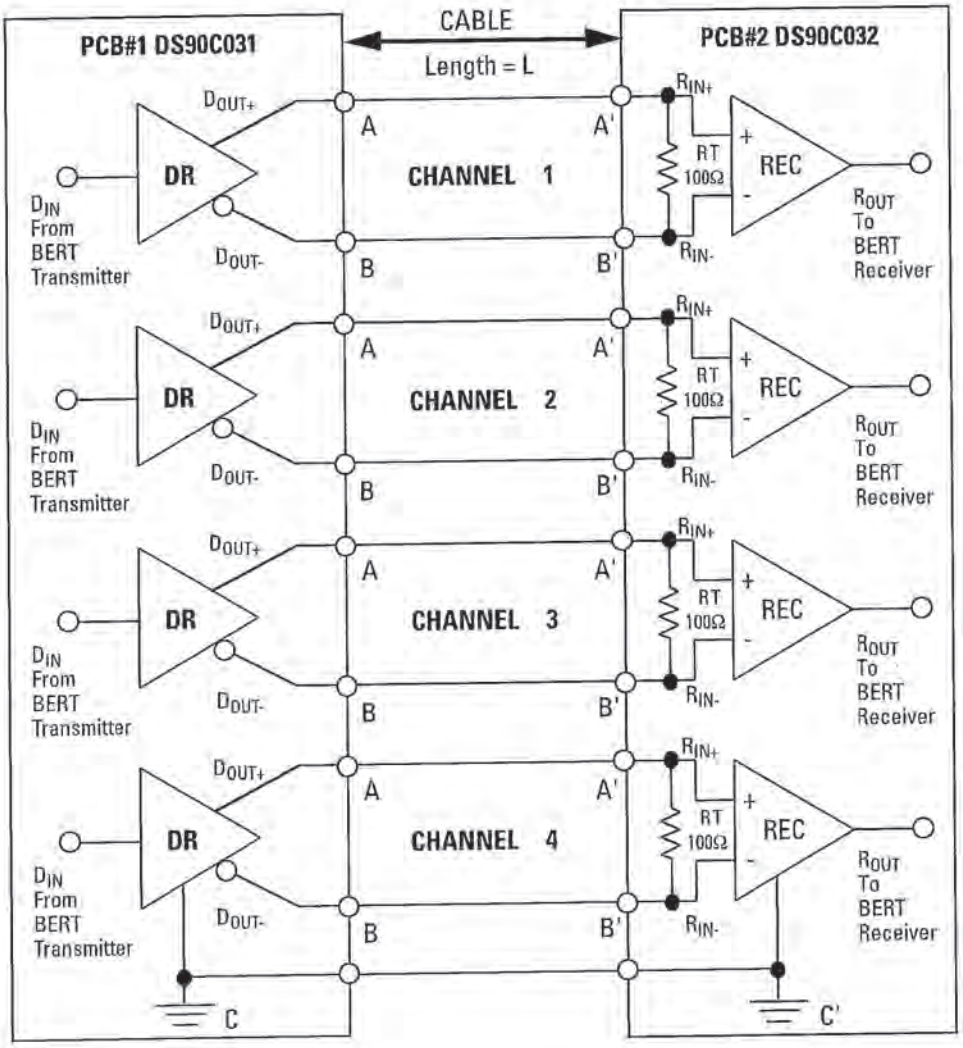
5.5.3 BER Test Circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in the next figure. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential-mode) 28 AWG stranded twisted pair cable (25 Pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report, cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.



LVDS BER Test Circuit

5.5.4 Test Procedure

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of 2^{15}-1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4-bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded which included: elapsed seconds, total bits transmitted and number of bit errors recorded. For the three tests documented next, a power supply voltage of +5.0V was used and the tests were conducted at room temperature.

5.5.5 Tests and Results

The goal of the tests was to demonstrate errors rates of less than 1×10^{-12} are obtainable.

TEST #1 Conditions:

Data Rate = 50Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

TEST #1 Results:

Total Seconds: 87,085 (1 day)
Total Bits: $1{,}723 \times 10^{13}$
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #2 Conditions:

Data Rate = 100Mbps
Cable Length = 1 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:

Total Seconds: 10,717 (~3 hr.)
Total Bits: 4.38×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

TEST #3 Conditions:

Data Rate = 100Mbps
Cable Length = 5 meter
PRBS Code = 2^{15}-1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

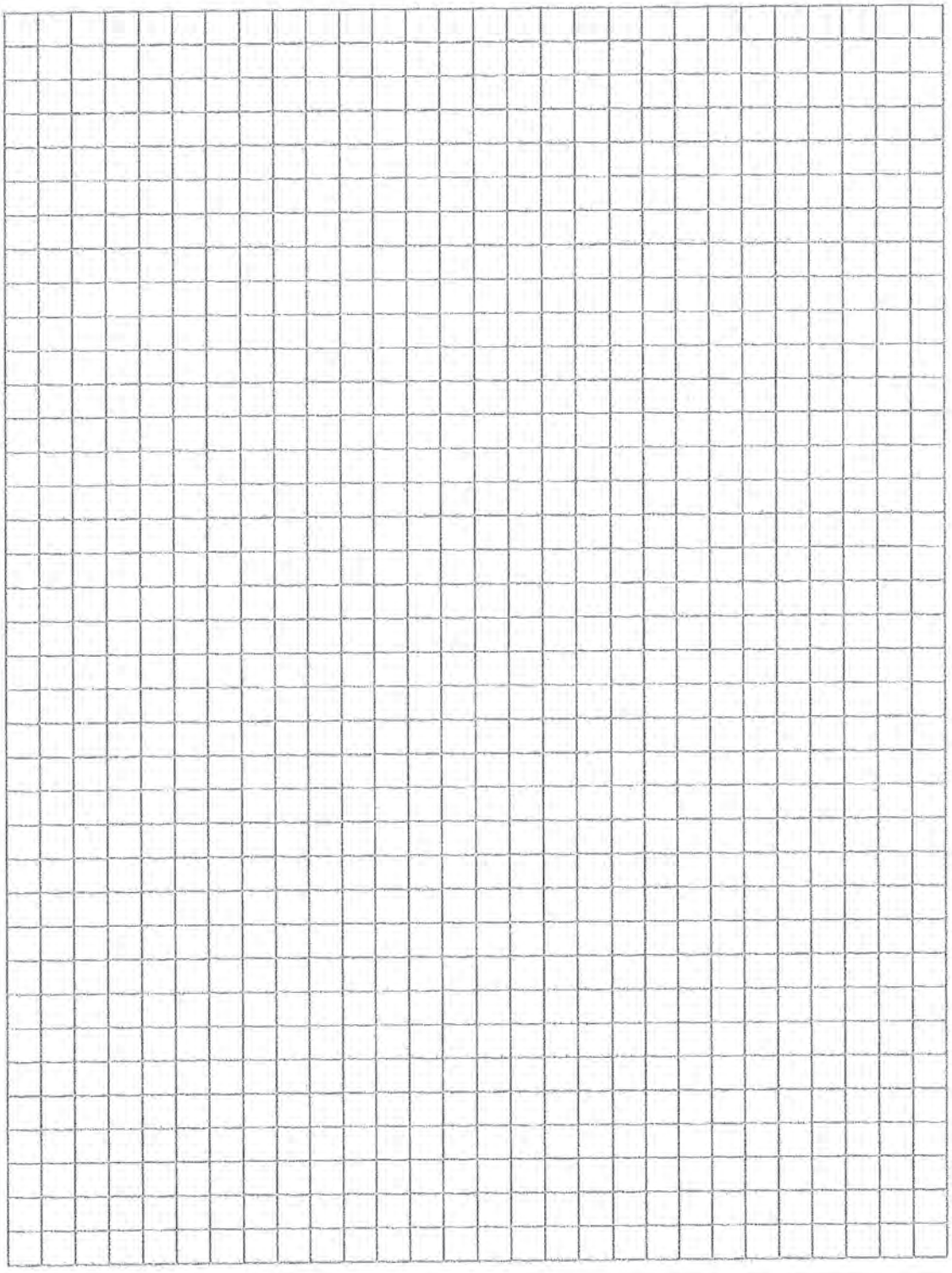
TEST #3 Results:

Total Seconds: 10,050 (~2.8 hr.)
Total Bits: 4×10^{12}
Errors = 0
Error Rate = $< 1 \times 10^{-12}$

5.5.6 Conclusions - BERT

All three of the tests ran error free and demonstrate extremely low bit error rates using LVDS technology. The tests concluded that error rates of $< 1 \times 10^{-12}$ can be obtained at 100Mbps operation across 5 meters of twisted pair cable. BER tests only provide a "Go — No Go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50Mbps to 100Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

NOTES



Backplane Design Considerations and Bus LVDS

Chapter 6

6.0.0 BACKPLANE DESIGN CONSIDERATIONS AND BUS LVDS

Many high-speed applications require more than just the ability to run point-to-point or from one driver to multiple receivers. Multiple driver(s) and/or receiver(s) on one interconnect is an efficient and common bus application. This requires a double termination of the interconnect to properly terminate the signal at both ends of the bus. Multipoint configurations offer an efficient balance between interconnect density and throughput. LVDS drivers are not intended for double termination loads, thus an enhanced family of devices was invented by National to bring the advantages of LVDS to bus applications.

For multidrop (with the driver located in the middle) and multipoint applications, the bus normally requires termination at both ends of the media. If the bus were terminated with 100Ω at both ends, a driver in the middle would see an equivalent load of 50Ω. Depending upon the load spacing, the effective impedance of the bus may drop further, and for signal quality reasons, the terminations may be as low as 60Ω. Again, a driver would see both resistors in parallel, thus a 30Ω load.

Standard (644) LVDS drivers have only 3.5mA of loop current. If these were used to drive the doubly terminated bus with a termination load of 30Ω, they would only generate a 105mV differential voltage on the bus. This small differential voltage is not sufficient when noise margins, reflections, over-drive and signal quality are taken into account. In fact, even doubling the drive is not enough for a heavily loaded backplane application.

Bus LVDS addresses the issue of driving a low impedance interconnect by boosting its driver current to about 10mA. This means that into a load as low as 30Ω, a 300mV differential signal is maintained. Thus, LVDS-like signaling with all of its benefits is obtained in doubly terminated bus applications.

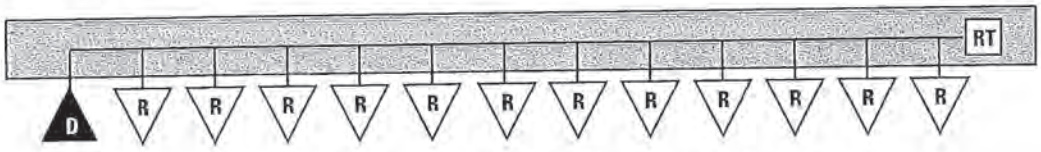
6.1.0 CONFIGURATIONS

Backplanes present special challenges to data transmission systems. This is due to the variety of interconnections (multidrop, multipoint, and switch fabrics) and also the close spacing of the loads. For these very reasons, National invented the Bus LVDS family of interface devices to extend the benefits of LVDS into backplane applications which commonly require two terminations.

There are a number of ways of implementing high-speed backplanes. Each of these ways of implementing a backplane has advantages and disadvantages.

6.1.1 Multidrop (Single Termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that the driver is restricted to be located at one end of the bus and the other end is terminated. This configuration is useful for data distribution applications and may employ standard LVDS or Bus LVDS devices.



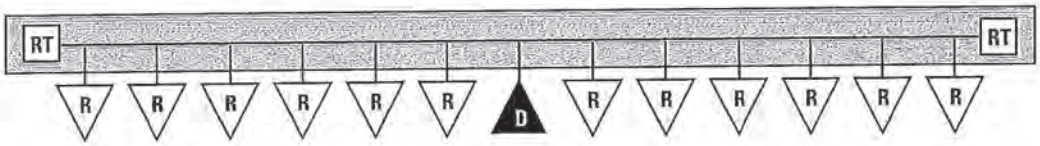
Multidrop Application with a Single Termination

This architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces) which in many cases reduces the stack up of the backplane to fewer layers.

A disadvantage of this configuration is the restricted location of the driver, and (if required) complexity of a back channel (communication path from the loads back to the source).

6.1.2 Multidrop (Double Termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that with Bus LVDS, the driver can be placed anywhere in the multidrop bus and the bus is terminated at both ends.

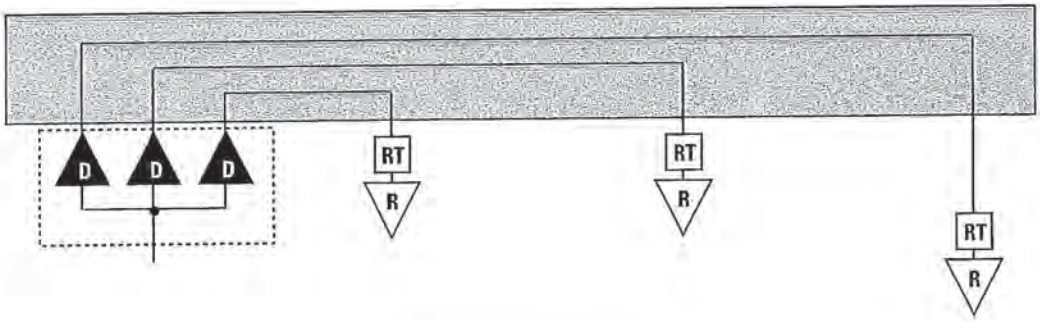


Multidrop Application with Double Termination

Again, this architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces). The advantages and disadvantages are the same as those discussed in 6.1.1.

6.1.3 Data Distribution with Point-to-Point Links

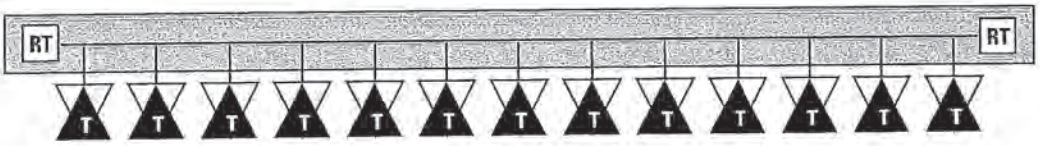
A distribution amplifier can also be used to buffer the signal into multiple copies which then drive independent interconnects to their loads. This offers optimized signal quality, the capability to drive long leads (long stub) to the loads, at the expense of interconnect density.



Data Distribution Application

6.1.4 Multipoint

The multipoint bus requires the least amount of interconnect (routing channels & connector pins), while providing bi-directional, half-duplex communication.



Multipoint Application

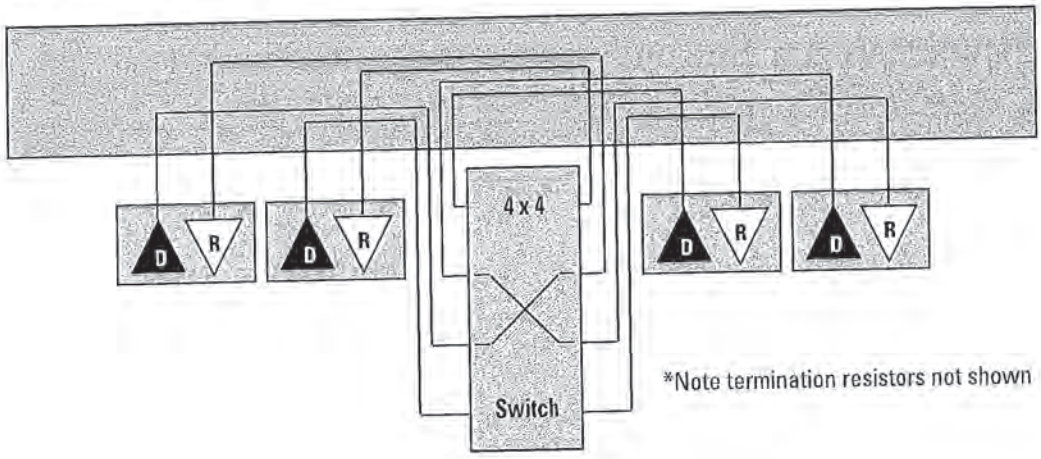
However, on this type of bus, there can only be one transaction at a time. Thus, a priority and arbitration scheme are typically required. These may be protocol or hardware solutions, depending upon the application.

6.1.4 Switch Matrix

Switch busses are growing in popularity for systems that require the very highest throughput possible. It is possible to have simultaneous transactions occurring on the switch bus at the same time and it has the cleanest electrical signal path of all the bus options (multidrop and multipoint, due to the no-stub effect).

The disadvantage of this type of scheme is that interconnect density increases with the number of loads, and also the complexity of the central switching card.

The switch application, due to its inherent optimized signal quality, is commonly used for links running hundreds of megabits per second into the Gigabit per second range. The top speed tends to be limited by the bandwidth of the interconnect.



Switch Application

6.2.0 BUS LVDS

6.2.1 System Benefits of Bus LVDS

There are numerous system benefits to using Bus LVDS over other technologies that have historically been used for bus interconnect. Many of these advantages are discussed next, but can be summed up with "Gigabits @ milliwatts!"

6.2.2 High-Speed Capability

Bus LVDS is capable of driving a multidrop or multipoint bus at high-speeds – for example:

- at 155Mbps across a 20 slot multipoint FR4 backplane
- at 400Mbps across a 10 slot multidrop FR4 backplane
- at 66MHz with ultra-low skew clock buffers
- at 800Mbps for point-to-point links

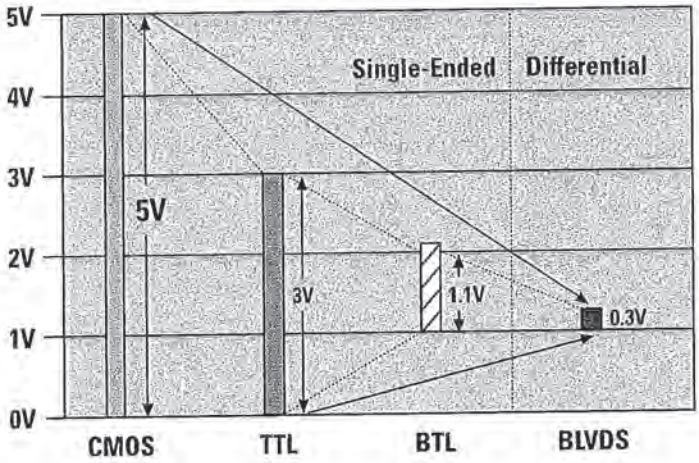
Previously, this has only really been achievable with the more costly high-speed ECL products. These present a translation challenge between common TTL devices and ECL drivers, and also power supply/termination problems. Other single-ended technologies were limited to sub 100MHz applications and presented tough termination and power dissipation problems. For a detailed comparison of back-plane technologies, please refer to *National Application note # 1123 – Sorting out Backplane Driver Alphabet Soup.*

6.2.3 Low Power

Bus LVDS switches an interconnect with only 10mA of loop current. This is much less than other high performance bus technologies that use large amounts of current (as much as 80mA in the case of BTL and 40+mA for GTL) to switch a bus with an incident wave. Typically, the load power for Bus LVDS is only 2.5mW. The current-mode drivers tend to offer low power dissipation, even at high data signaling rates. Lastly, with the low swings required, the supply rails may be less than 5V, 3.3V or even 2.5V. These three reasons make LVDS and Bus LVDS components extremely low power.

6.2.4 Low Swing/Low Noise/Low EMI

Bus LVDS uses a low swing differential signal. This small balanced signal transition generates small EMI, and the current-mode driver limits spiking into the supply rails. These reasons make the LVDS driver capable of running at better than 10x the frequency of TTL at lower EMI levels.



Comparison of Voltage Swings for Various Backplane Technologies

CMOS and TTL technologies use a large swing and often large currents in order to switch a bus. This switching can cause ringing and undershoot which can be a large contributor to system EMI.

BTL addressed this noise issue by reducing its output swing to just 1V. However, it still uses large amounts of current to switch the bus with an incident wave (80mA typical) and still uses the single-ended approach with limited noise margins and a complex termination scheme.

As we have seen, Bus LVDS uses only 10mA to switch the bus with an incident wave, is low swing (300mV typical) and is differential. We saw in Section 4.3.2 how differential signaling can help substantially reduce system EMI. The small swing also provides the high-speed capability while consuming minimal power.

6.2.5 Low System Cost

All of National's Bus LVDS products are implemented in a core CMOS technology which allows for low manufacturing cost and the ability to integrate more functionality onto one piece of silicon. By putting the coding, clock recovery, and other PHY/LINK layer digital functions into the interface device, ASIC complexity and risk is greatly reduced. Immense system savings can be obtained through the use of the Serializer and Deserializer chipsets. Connectors, cable size and cost may be reduced. In most cases, these savings more than compensate for the interface silicon cost!

6.2.6 System Benefits

Besides the cost effectiveness of using Bus LVDS, there are also other system savings in using Bus LVDS:

- **Low Power**
  - Its CMOS design helps reduce the cost of system power supplies and cooling, enabling fan-free applications!
- **Simple Passive Terminations**
  - A bus can be implemented using only discrete components for termination. Other high-speed bus technologies such at GTL, BTL and ECL require active termination devices and/or odd ball supply rails (+1.5V, +2.1V for example) which add to system cost and power distribution complexity.
- **Serialization**
  - National's Bus LVDS portfolio consists of bus-able serializers and deserializers which reduce system interconnect and connector size.
- **Low Noise**
  - The low noise characteristic of Bus LVDS help with the limitation of EMI within a system which can help with system cycle times and system cost reductions.

6.3.0 BACKPLANE DESIGN CONSIDERATIONS

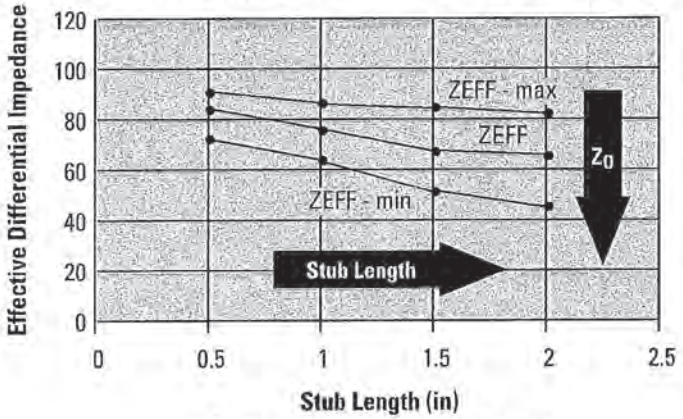
Prior to the start of any system design, the following methodology should be used.

1. System design starts with a solid power and ground distribution system. When this is left to the last step, it tends to be the source of noise and EMI problems.
2. Next, consider the transmission line configuration and layout. Optimize paths to provide the best signal quality. Locating certain devices close to the connector location and other devices (potential noise sources) far away is one way to do this. Give priority to the layout of the transmission line traces to avoid unnecessary via and in-balances.
3. Complete the remaining digital design.
4. Always review the completed layout.

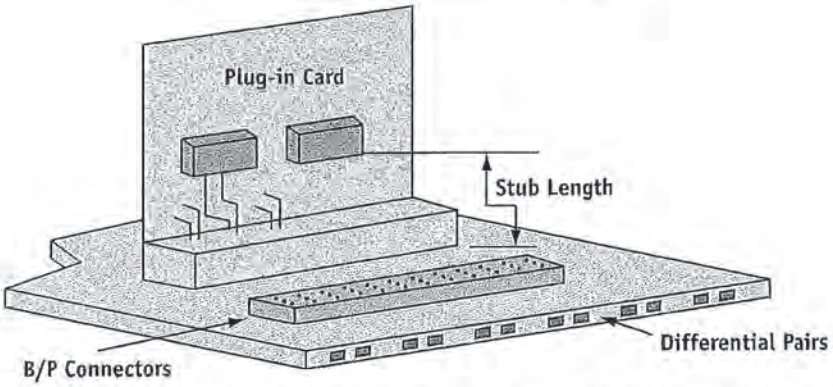
6.3.1 Loading Effects

The next figure shows the differential bus with one card plugged in. The card adds a load to the bus which is mainly composed of a bulk capacitance load (CD) resulting from the connector (2-3pF), the PCB trace (2-3pF) and the device (4-5pF), for a total load of about 10pF. Limit the number of vias on the card's stub to minimize capacitance loading. Also, keep stub lengths as short as possible. These two tips will help to maintain a high "loaded" bus impedance that will increase noise margins.

The TDR Simulated Differential Impedance of 20 Slot, Full Loaded BLVDS Backplane with Differential Z_0 = 130Ω



Source: NESA BLVDS WhitePaper

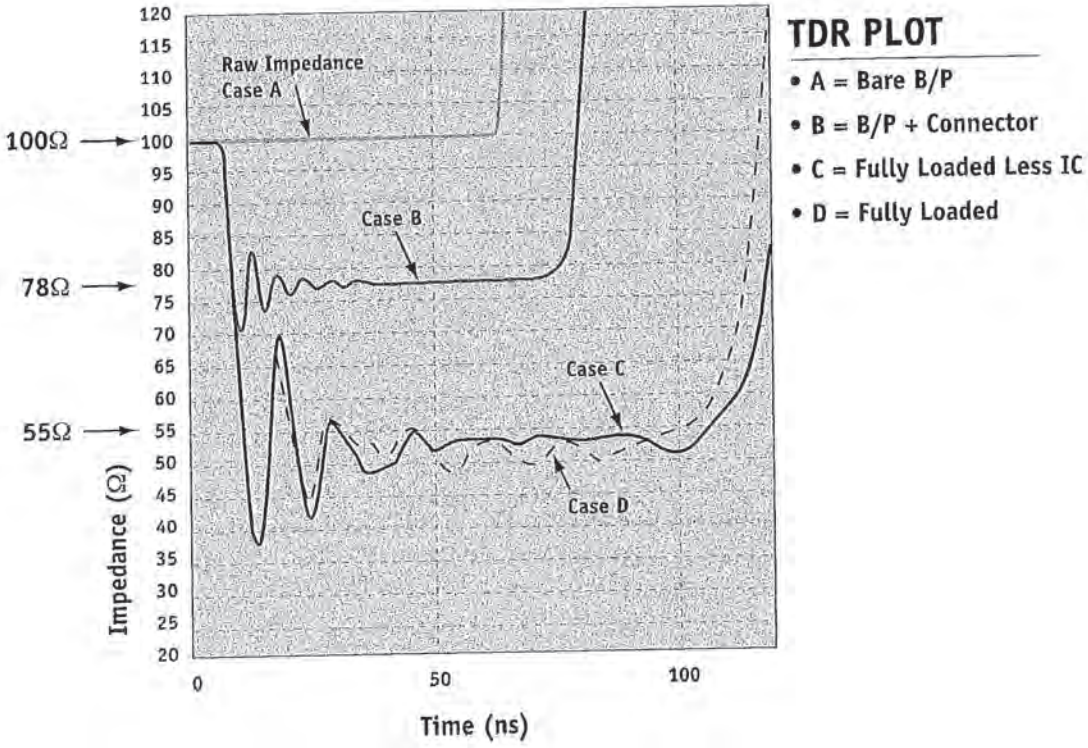


BLVDS is capable of operating in wild card configurations! Depending upon system noise margin goals, full card loading is NOT required. Termination selection is a bit tricky, but should be matched to a fully loaded case (or slightly higher). Waveshape is good even for half loaded or section loaded busses! Single-ended technologies can not support this feature due to noise margin violations.

The next figure provides a TDR simulation of a backplane impedance vs. loading.

- Case A shows the raw traces only (no via)
- Case B inserts the backplane connectors
- Case C adds all the cards into the bus, note that the cards do not include the device
- Case D adds the device to the card, thus it is a fully loaded system

Notice that about 50% of the loading is due only to the backplane connectors and their vias. Also notice how the velocity of the signal is slowed by the loading. This final value is equal to the parallel loading of the two 56Ω termination resistors.



6.3.2 Bus Termination

Termination is required for two reasons:

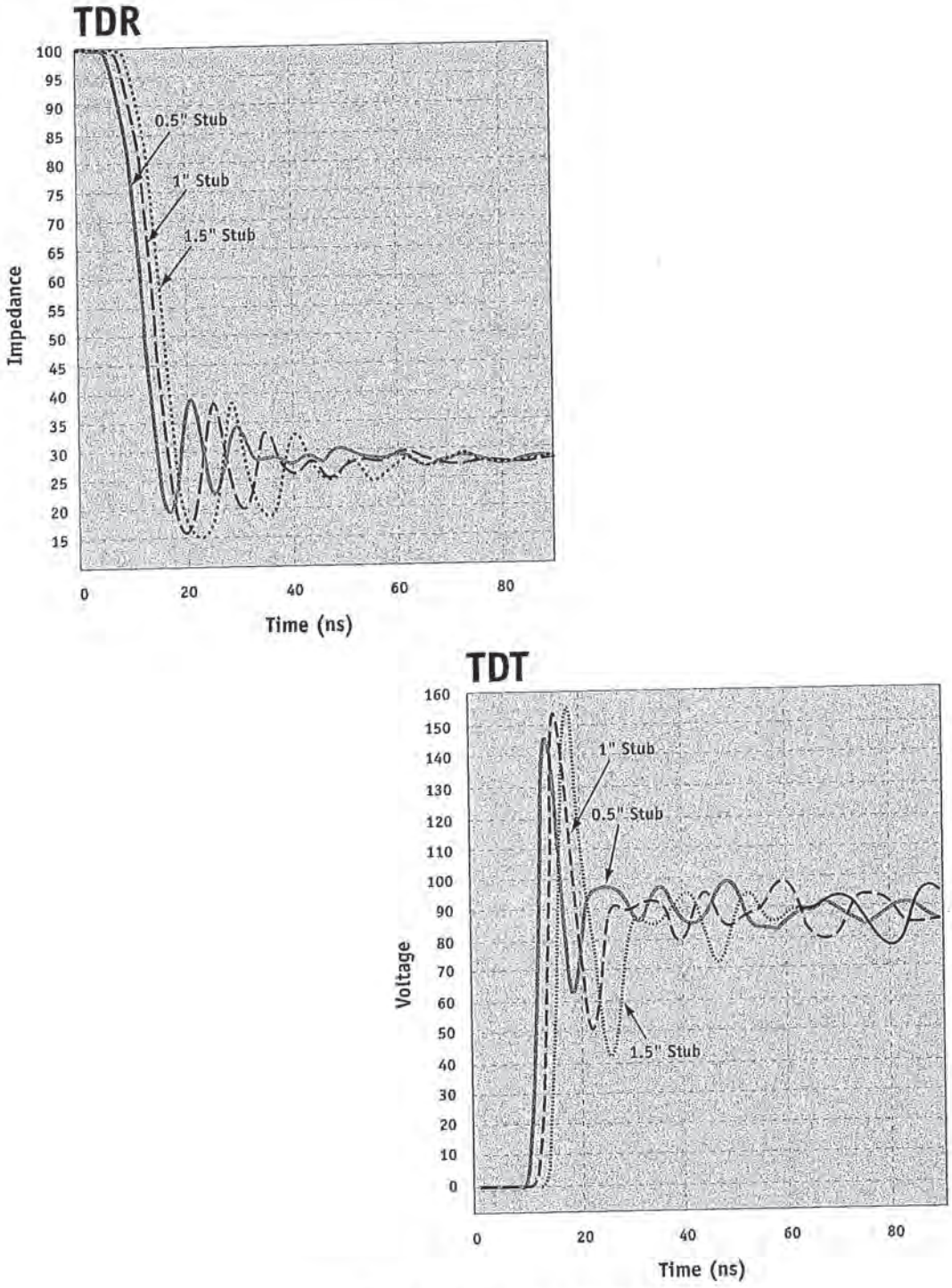
1. Current-mode drivers require the resistor to complete the current loop.
2. BLVDS edge rates are fast and the interconnect will act as a transmission line, therefore terminations are needed to limit reflections.

BLVDS only requires a simple termination of a single surface mount resistor across the line at each end of the bus for multipoint applications. There is no need for a special V_T rail or active termination devices, as with single-ended technologies (TTL/BTL/GTL). The resistor should be equal to or slightly greater than the loaded differential impedance of the line. Typically, it is located at both ends of the backplane depending upon the configuration/application. (See also 6.3.5 on Failsafe Biasing).

6.3.3 Stub Length

Stubs - one golden rule: **The shorter the better!**

A long stub adds to the capacitive load, lowers the loaded impedance even more and tends to impact signal quality. For this reason, stub interconnect should be a microstrip and the number of vias (0-1 is best) should be limited. The graph below is from the NESA White Paper on BLVDS (available from www.national.com/appinfo/lvds/) and illustrates how increasing stub length lowers the loaded impedance. Stub length should be typically 1-1.5" or less.

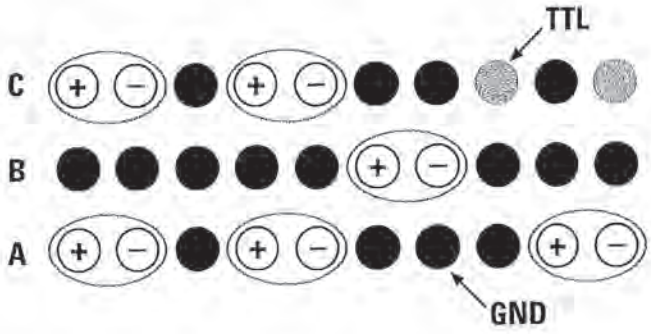


300ps Input Signal vs 0.5"/1.0"1.5" Stub

6.3.4 Connectors

Connectors are a complex topic and are the subject of many heated debates at standard committee meetings. There are two basic types: standard matrix based connectors (3 rows of 32-pins) and special connectors. The special connectors may be optimized for differential signals or may use elaborate techniques to clamp to the PCB. The elaborate connectors tend to avoid via structures and thus offer the highest bandwidth. They are also very application specific and tend to be rather expensive.

More common is the use of standard connectors for a mix of differential, power, ground and single-ended connections (see below). The graphic below shows a variety of pinout recommendations for single-ended and differential options.



Typical Connector Pinouts

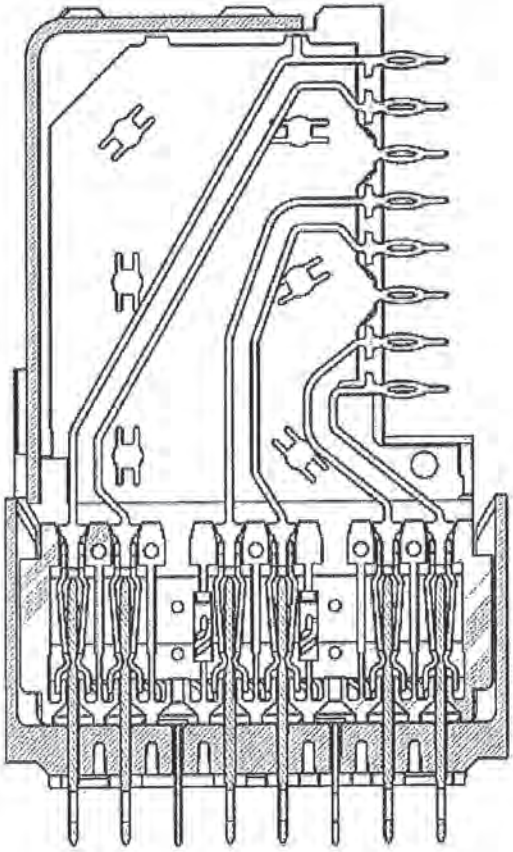
For differential lines in a matrix (single-ended) connector, adjacent pins in a row tend to be better as the electrical length are the same. The row with the shorter path provides a better path over the longer row also.

Ground signal assignment can be used to isolate large swing (TTL) signals from the small-swing lines as shown above.

Connector Example: Teradyne VHDM High-Speed Differential Connector

This is a differentially optimized high-density connector for applications into the Gigabit per second range. It is offered in both an 8 row (which provides 3 differential pairs) and a 5 row (which provides 2 differential pairs) configurations. The 8 row connector can coexist with the basic 8 row VHDM single-ended connector and also power/ground contacts. Shielding is provided between wafers providing excellent isolation of signal contacts. The backplane layout is also improved over earlier generations and the new footprint now supports wider traces (10mils) to be routed through the pin field easing backplane design. The backplane side of the connector accepts either the single-ended or differential versions of VHDM. Skew has been minimized within the pair and also the pairs are routed together (see next drawing). This is an example of a high-throughput differential optimized connector that provides excellent signal quality. For details, please visit the Teradyne website at:
www.teradyne.com/prods/bps/vhdm/hsd.html

Testing is planned at National for the Summer of 2000 to evaluate this connector with various LVDS devices. Check our LVDS website for the results of this testing to be available late Summer 2000.



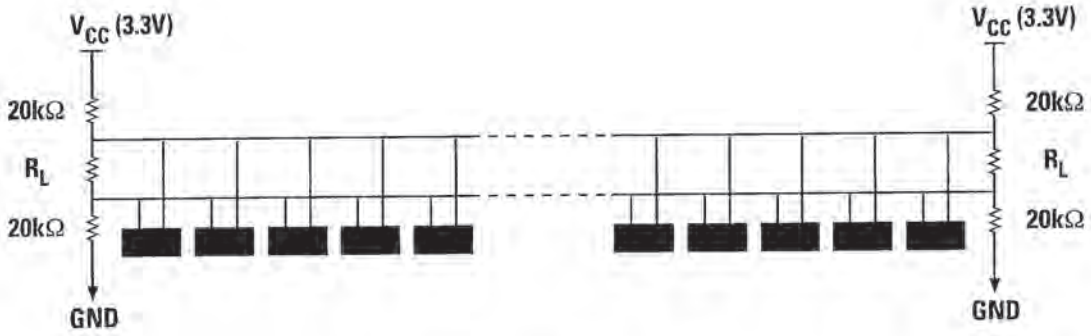
Cross Section of VHDM HSD
(Graphic courtesy of Teradyne)

6.3.5 Failsafe Biasing

Failsafe biasing may be required if a known state is required on the bus when any of the following conditions occur:

- All drivers are in TRI-STATE® – common in multipoint applications.
- All drivers are removed or powered-off

If this is the case, additional biasing (beyond the internal failsafe biasing of the receivers) may be provided with a failsafe biasing (power) termination as shown in the next figure.



Multipoint Bus with Failsafe Bias

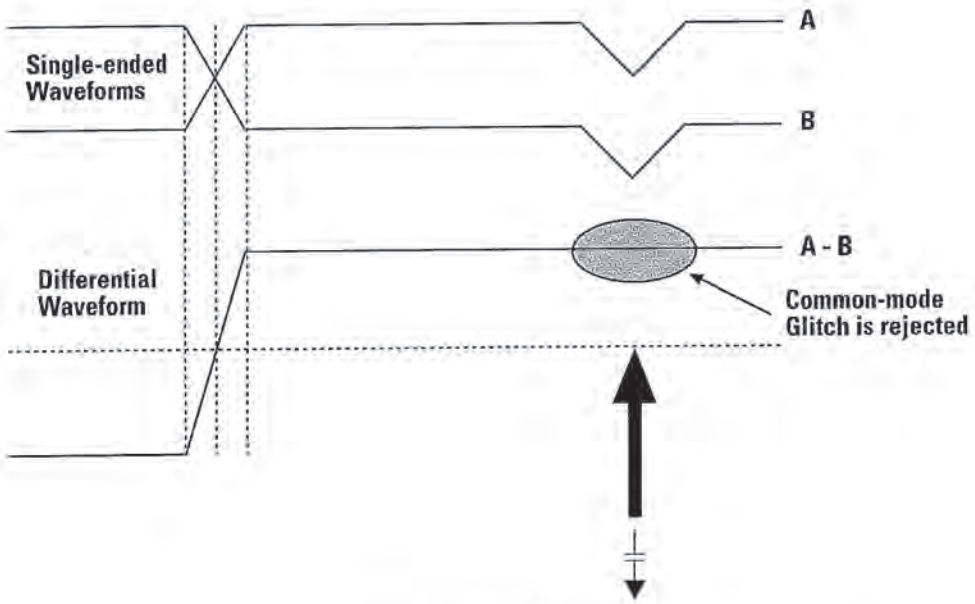
In selecting failsafe resistor values note the following:

- The magnitude of the resistors should be 1 to 2 orders higher than the termination resistor, to prevent excessive loading to the driver and waveform distortion
- The mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common-mode shift from occurring between active and TRI-STATE® (passive) bus conditions
- The pull-up and pull-down resistors should be used at both ends of the bus for quickest response
- Note that signal quality is reduced as compared to active driving (on/on)
- See Chapter 4 for equations for selecting failsafe biasing resistors

6.3.6 Hot Plugging/Live Insertion

Live Insertion, or Hot Swapping, is of particular importance to the telecommunications marketplace. In these applications, it is critical that maintenance, upgrading and repair can be performed without shutting down the entire system or causing disruption to the traffic on the backplane. BLVDS's wide common-mode range of ±1V plays a key role in supporting this function. Upon insertion of a card into a live backplane, the occurrence of abnormalities on the signals are common on both signals, thus data is not impacted. This allows for safe hot swapping of cards, making the systems robust and reliable.

Lab testing done in the National LVDS Interface Lab has shown zero-bit errors while plugging in or removing cards from an active bus (BERT test). During the test, up to four cards were inserted at once without an error! This is due to the fact that the differential lines equally load the active line on contact and any glitch seen is a common-mode modulation that is ignored by the receivers.



Live Insertion Waveforms

However, standard power sequencing is still recommended to ensure proper biasing of the devices (substrate). For insertion, the following sequence should be guaranteed by hardware design:

1. Ground
2. Power
3. I/O pins

For removal, the reverse order is recommended (3-2-1). This sequence can be supported a number of ways. Staggered power pin connectors may be employed (available from multiple sources and even compatible with many matrix connector styles). Multiple connectors are also commonly used. A D_{IN} connector for the I/O, and "Jack" like connectors for power and ground is one approach. Yet another option uses card edge contact on the rails to establish a GND bias when the card is first inserted into the card rail.

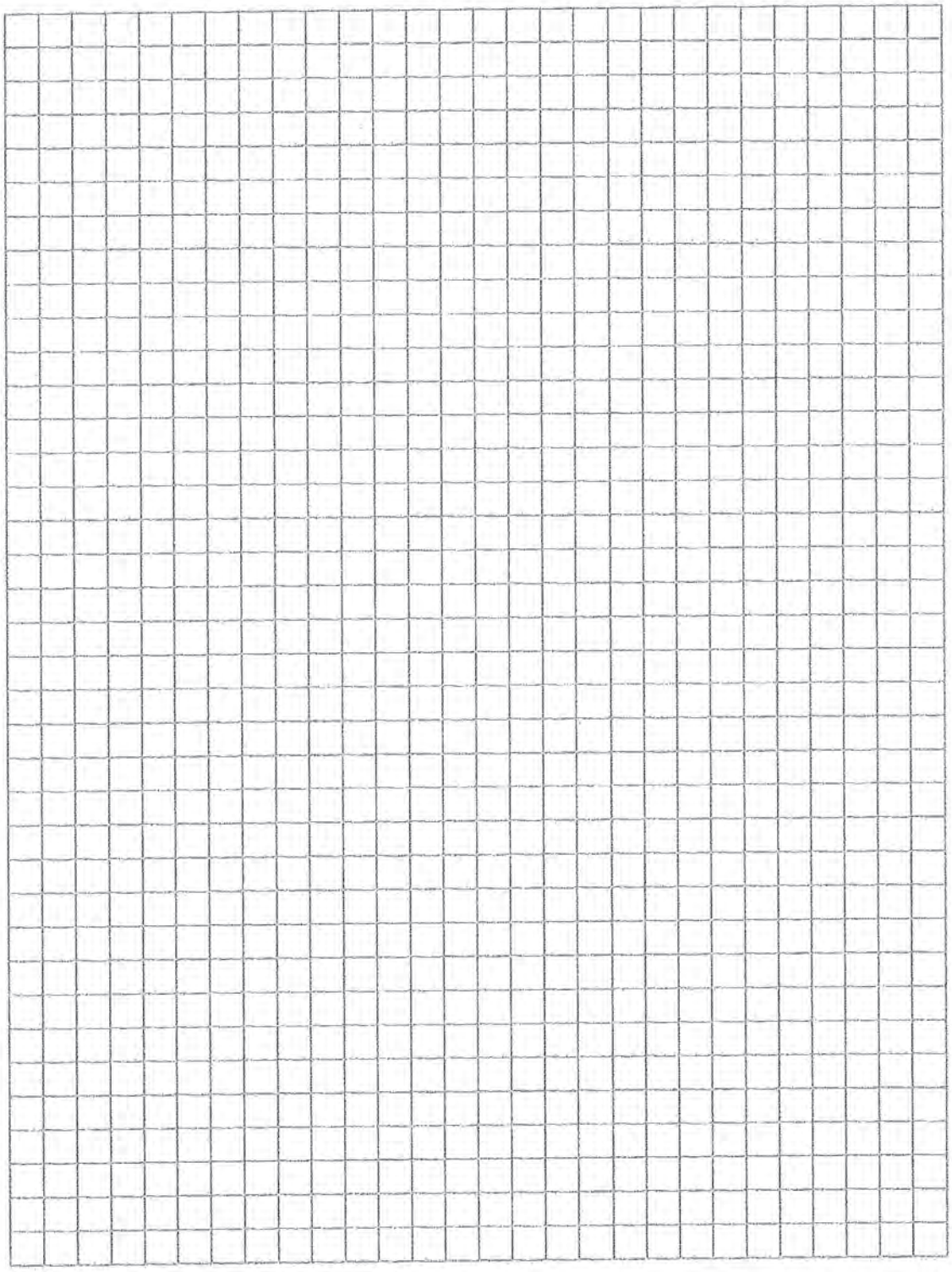
6.4.0 ADDITIONAL INFORMATION

Detailed backplane design information is available from our website in the form of white papers and also application notes. National has also teamed up with NESA (North East System Associates Inc.) and jointly published a number of white papers and conference papers. Recent papers are available from both websites:

www.national.com/appinfo/lvds/

www.nesa.com

NOTES



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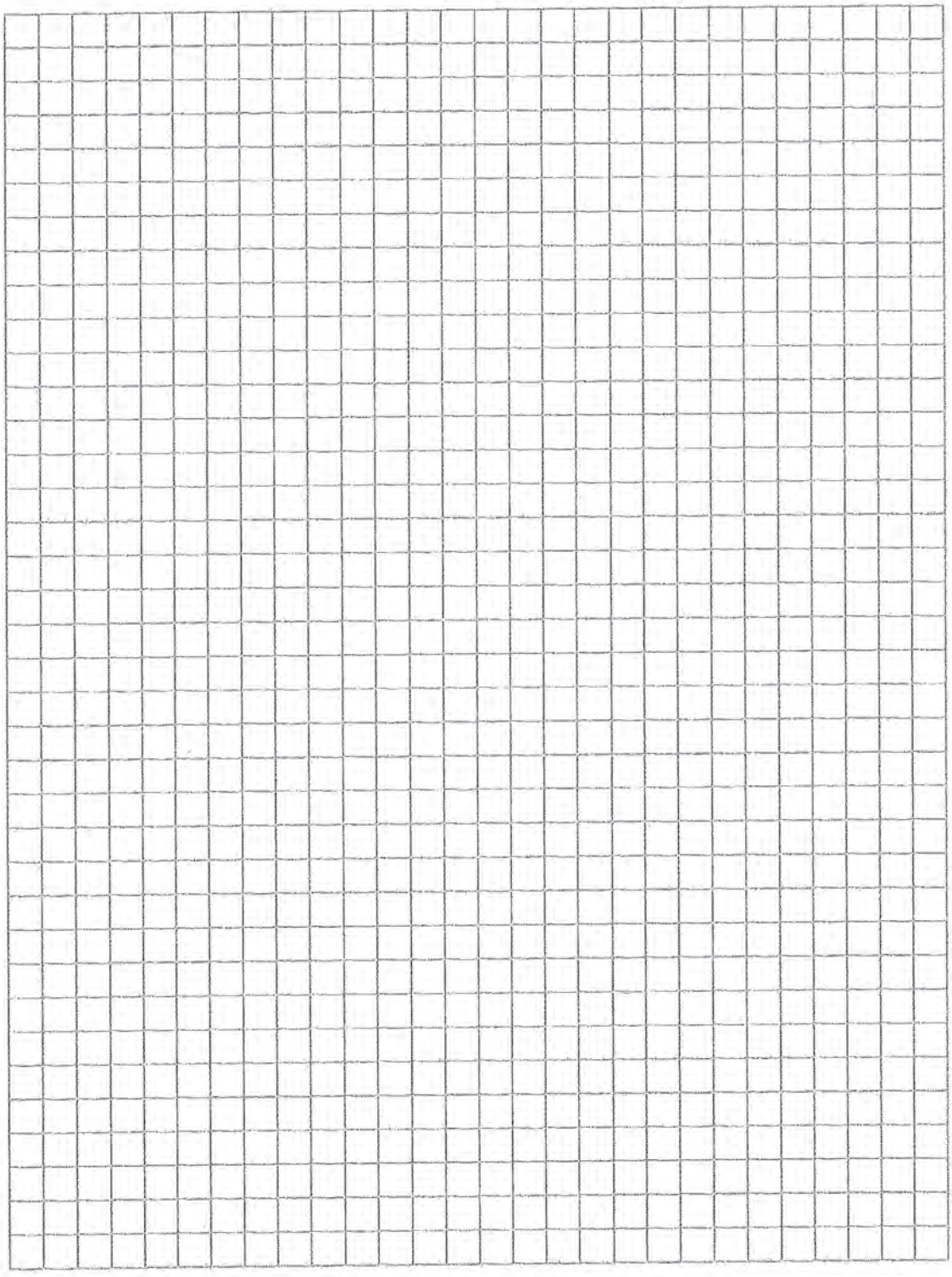


LVDS Evaluation Kits

Chapter 7

7.0.0 LVDS EVALUATION BOARDS AND EVALUATION KITS

Evaluation kits, offered at a nominal cost, demonstrate the LVDS Physical Layer Interface devices. Please consult the LVDS website for a link to the page that provides updated information on the Evaluation Kits. The "Evaluation/Demo Board" page contains:

- LVDS Family (LVDS, Channel Link, Bus LVDS, etc)
- A short description of the board or kit
- A list of the NSID(s) (part numbers) that are on the PCBs
- The kit's order number (Order Number)
- An update/revision/errata link (if applicable)

Also note that on selected kits, the user's manual for the specific kit can now be downloaded directly from this page. This allows the user to determine exactly the content, capability, and features of the kit prior to purchasing the kit.

7.1.0 LVDS KITS - SHORT DESCRIPTIONS

7.1.1 The Generic LVDS Evaluation Boards

The Generic LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over PCB trace, twisted pair cable, or custom transmission medium. Flow through LVDS quad drivers and receivers are used on the board. They can represent the LVDS I/O characteristics of most of National's 3.3V LVDS devices. Included in the latter part of this section is the complete user's documentation for the new LVDS47/48EVK. See Section 7.2.0 below.

While supplies last, the original generic LVDS evaluation board is available as both an assembled kit (LVDSEVAL-001) and also as an un-stuffed PCB (order as a literature piece, LIT# 550061-001). This PCB accommodates a SCSI-2 50 pin cable interface.

7.1.2 Channel Link Evaluation Kits

These boards are fully populated. TTL signals are accessed through IDC connectors on the transmitter and receiver boards. The boards are interconnected via a ribbon cable that can be modified for custom lengths for the 21 & 28-bit chipsets. The 48-bit chipset features a 3M MDR cable and connector system. These evaluation boards are useful for analyzing the operation of National's high-speed Channel Link devices.

7.1.3 Bus LVDS Evaluation Kits

These boards are fully populated. Currently a mini backplane kit is offered (different RX device options available). A stand-alone test system is also offered. The BLVDS03 kit provides a PRBS generator that provides data to the BLVDS Serializer and also checks the received data from the BLVDS Deserializer. This kit only requires a power supply voltage. These evaluation boards are useful for analyzing the operation of National's New Bus LVDS SER/DES devices.

7.1.4 Special Function LVDS Evaluation Kits

New special function LVDS/BLVDS devices are being developed for special applications. The first EVAL KIT is for the DS90CP22 2x2 800Mbps Digital Crosspoint Switch. Check our website for the latest information on new kits.

7.1.5 FPD-Link Evaluation Kits

These boards are fully populated. TTL signals are accessed through IDC connectors on the transmitter and receiver boards. The boards are interconnected via a cable. These evaluation boards are useful for analyzing the operation of National's high-speed FPD-Link and LDI devices. Current information on the FPD Link Evaluation Kits can be accessed from the FPD website at: **www.national.com/appinfo/fpd/**

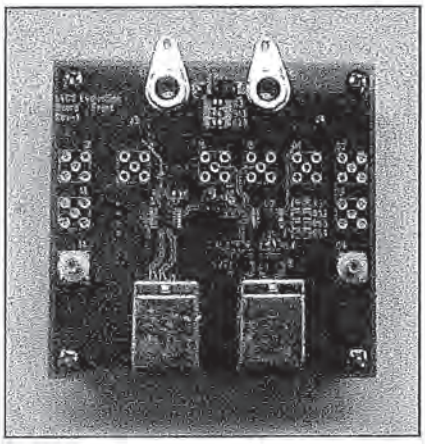
7.1.5 Related Parts

- Use the DS90C031/032 on the original generic LVDS evaluation board (LVDSEVAL-001) to represent the LVDS I/O characteristics of all 5V drivers/receivers, 5V Channel Link, and 5V FPD-Link devices.
- Use the DS90LV047A/048A on the new generic LVDS evaluation board (LVDS47/48EVK) to represent the LVDS I/O characteristics of 3V Channel Link, 3V FPD-Link, and other 3V devices.

The remainder of this chapter explains the operation of the new generic LVDS Evaluation Board.

7.2.0 THE GENERIC LVDS EVALUATION KIT – THE LVDS4748EVK

7.2.1 The Flow Through LVDS Evaluation Board

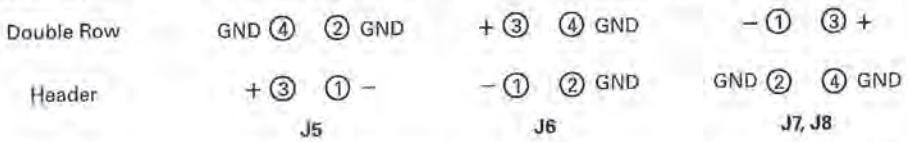


The Flow Through LVDS Evaluation Board

The Flow Through LVDS Evaluation Board is used to measure LVDS signaling performance over different media. Individual LVDS channels can be evaluated over a PCB trace, RJ45 connector and CAT5 UTP cable, or custom transmission medium. Though LVDS quad drivers and receivers are used on the board, they can represent the standard LVDS I/O characteristics of most of National's LVDS devices. We can also use the DS90LV047A/048A to represent the LVDS I/O characteristics of 3V Channel Link and 3V FPD-Link devices.

7.2.2 Purpose

The purpose of the Low Voltage Differential Signaling (LVDS) Evaluation Printed Circuit Board (PCB) is to demonstrate the line driving capability of LVDS technology across a short PCB interconnect, and also across a variable length of RJ45 cable. Probe points for a separate driver and a separate receiver are also provided for individual line driver or receiver testing. The part number for the Evaluation Kit is LVDS47/48EVK. In this application note, the following differential signal nomenclature has been used: "Jx-3" represents the true signal and "Jx-1" represents the inverting signal. On the PCB, the true signal is represented by a '+' and the inverting signal is on the adjacent header pin as shown below.



The two adjacent ground pins are there to view the true or inverting signal single-endedly. Input signals are represented with an "I" while receiver outputs are represented with an "O."

7.2.3 Five Test Cases

Five different test cases are provided on this simple 4 layer FR-4 PCB. Each case is described separately. The five test cases are shown in the following figure.

LVDS Channel #1A: LVDS Line Driver
This test channel provides test points for an isolated driver with a standard 100Ω differential termination load. Probe access for the driver outputs is provided at test points on J5-1 and J5-3. The driver input signal (I1) is terminated with a 50Ω termination resistor (RT1) on the bottom side of the PCB.

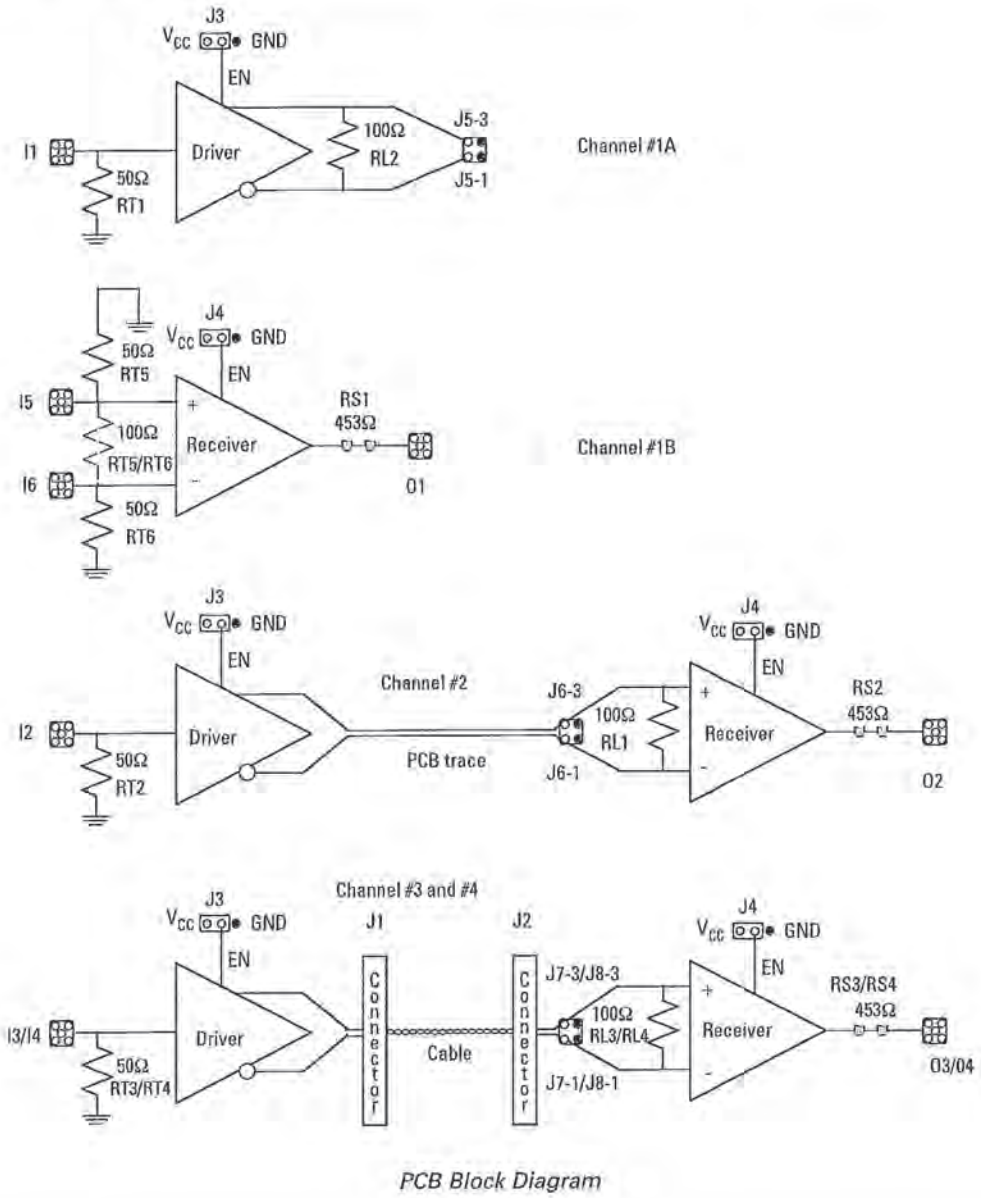
LVDS Channel #1B: LVDS Receiver
This test channel provides test points for an isolated receiver. Termination options on the receiver inputs accommodate either two separate 50Ω terminations (RT5 and RT6) (each line to ground) or a 100Ω resistor connected across the inputs (differential). The first option allows for a standard signal generator interface. Input signals are connected at test points I5 (R_{IN-}) and I6 (R_{IN+}). A PCB option for a series 453Ω resistor (RS1) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is with two separate 50Ω terminations (RT5 and RT6) and without the series 453Ω resistor (RS1) for use of high impedance probes. The receiver output signal may be probed at test point O1.

LVDS Channel #2: PCB Interconnect
This test channel connects Driver #2 to Receiver #2 via a pure PCB interconnect. A test point interface of the LVDS signaling is provided at test point J6-1 and J6-3. The driver input signal (I2) is terminated with a 50Ω termination resistor (RT2) on the bottom side of the PCB. The receiver output signal may be probed at test point O2. A PCB option for a series 453Ω resistor (RS2) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is without the series 453Ω resistor for use of high impedance probes. A direct probe connection is possible with a TEK P6247 differential probe high impedance probe (>1GHz bandwidth) on the LVDS signals at test points J6-1 and J6-3. This channel may be used for analyzing the LVDS signal without the bandwidth limiting effects of a cable interconnect.

LVDS Channel #3: Cable Interconnect
This test channel connects Driver #3 to Receiver #3 via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I3) is terminated with a 50Ω termination resistor (RT3) on the bottom side of the PCB. LVDS signals are probed via test points on J7. The receiver output signal may be probed at test point O3. A PCB option for a series 453Ω resistor (RS3) is also provided in case 50Ω probes are employed on the receiver output signal (see options section). The default setting is without the series 453Ω resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1GHz bandwidth) on the LVDS signals at test point J7-1 and J7-3.

LVDS Channel #4: Cable Interconnect

This test channel connects Driver #4 to Receiver #4 also via the cable interconnect. A test point interface is provided at the receiver input side of the cable. The driver input signal (I4) is terminated with a 50Ω termination resistor (RT4) on the bottom side of the PCB. LVDS signals are probed via test points on J8. The receiver output signal may be probed at test point O4. A PCB option for a series 453Ω resistor (RS4) is also provided in case 50Ω probes are employed on the receiver output signal. The default setting is without the series 453Ω resistor for use of high impedance probes. A differential probe connection is possible with a TEK P6247 differential probe (>1 GHz bandwidth) on the LVDS signals at test point J8-1 and J8-3. This channel duplicates channel #3 so that it may be used for a clock function or for cable crosstalk measurements.

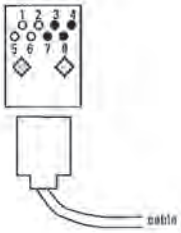


PCB Block Diagram

7.2.4 Interconnecting Cable and Connector

The evaluation PCB has been designed to directly accommodate a CAT 5 four twisted pair (8-pin) RJ45 cable. The pinout, connector, and cable electrical/mechanical characteristics are defined in the Ethernet standard and the cable is widely available. The connector is 8 position, with 0.10" centers and the pairs are pinned out up and down. For example, pair 1 is on pins 1 and 5, not pins 1 and 2 (see Figure below).

IMPORTANT NOTE: The 2 unused pairs are connected to ground. Other cables may also be used if they are built up.

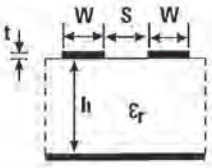


RJ45 Connector

7.2.5 PCB Design

Due to the high-speed switching rates obtainable by LVDS, a minimum of a four layer PCB construction and FR-4 material is recommended. This allows for 2 signal layers and full power and ground planes. The stack is: signal (LVDS), ground, power, signal.

Differential traces are highly recommended for the driver outputs and the receiver inputs signal (LVDS signals, refer to PCB layout between U1 and J1). Employing differential traces will ensure a low emission design and maximum common-mode rejection of any coupled noise. Differential traces require that the spacing between the differential pair be controlled. This distance should be held as small as possible to ensure that any noise coupled onto the lines will primarily be common-mode. Also, by keeping the pair close together the maximum canceling of fields is obtained. Differential impedance of the trace pair should be matched to the selected interconnect media (cable's differential characteristic impedance). Equations for calculating differential impedance are contained in National application note AN-905 for both microstrip and stripline differential PCB traces.



For the microstrip line, the differential impedance, Z_{DIFF}, is:

$$Z_{DIFF} \cong 2Z_O\,(1 - 0.48e^{-0.96S/h})\Omega$$

For the new evaluation board h = 24mils, S = 11mils and Z_O = 70Ω. Calculating the differential impedance, Z_{DIFF}, is:

$$Z_{DIFF} \cong 2Z_O\,(1 - 0.48e^{-0.96(11/24)})\Omega$$

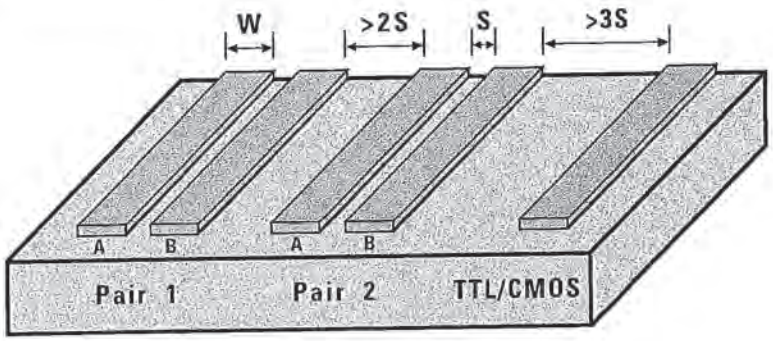
$$2\,(70)\,(0.69086)\Omega$$

$$96.72\Omega$$

Termination of LVDS lines is required to complete the current loop and for the drivers to properly operate. This termination in its simplest form is a single surface mount resistor (surface mount resistor mini-

mizes parasitic elements) connected across the differential pair as close to the receiver inputs as possible (should be within 0.5 inch (13mm) of input pins). Its value should be selected to match the interconnects differential characteristics impedance. The closer the match, the higher the signal fidelity and the less common-mode reflections will occur (lower emissions too). A typical value is 100Ω ±1%.

LVDS signals should be kept away from CMOS logic signals to minimize noise coupling from the large swing CMOS signals. This has been accomplished on the PCB by routing CMOS signals on a different signal layer (bottom) than the LVDS signals (top) wherever possible. If they are required on the same layer, a CMOS signal should never be routed within three times (3S) the distance between the differential pair (S). Adjacent differential pairs should be at least 2S away also.

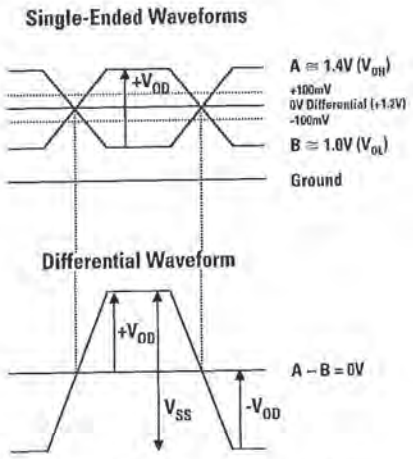


Pair Spacing for Differential Lines

Bypassing capacitors are recommended for each package. A 0.1 µF is sufficient on the quad driver or receiver device (CB1 and CB2) however, additional smaller value capacitors may be added (i.e. 0.001µF at CB21 and CB22) if desired. Traces connecting V_{CC} and ground should be wide (low impedance, not 50Ω dimensions) and employ multiple vias to reduce inductance. Bulk bypassing is provided (CBR1, close by) at the main power connection as well. Additional power supply high frequency bypassing can be added at CB3, CB13, and CB23 if desired.

7.2.6 Sample Waveforms from the LVDS Evaluation PCB

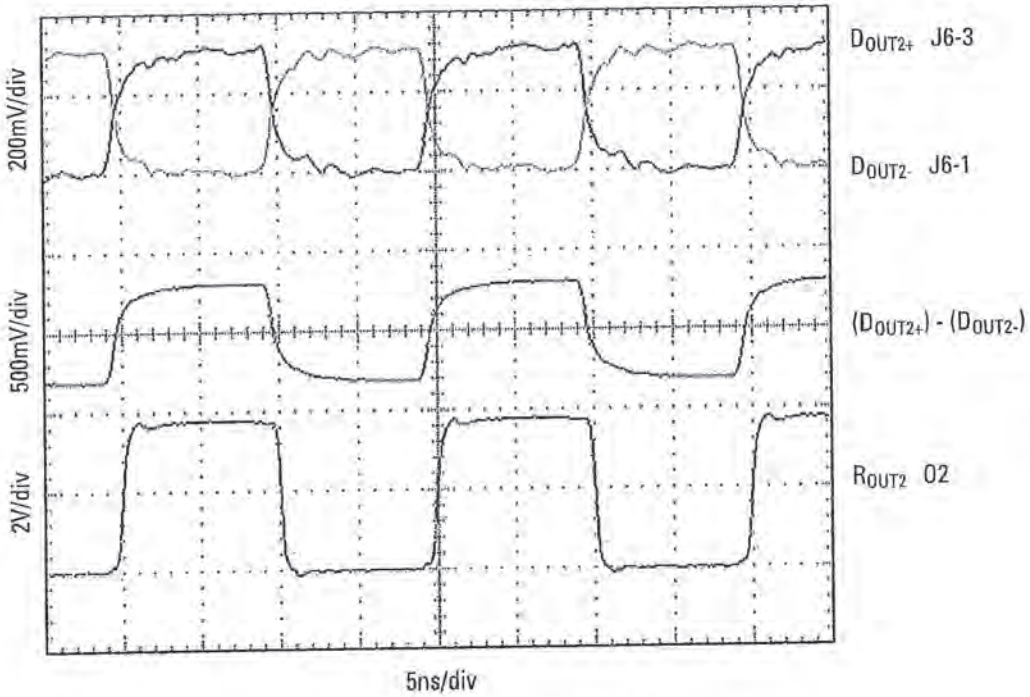
Single-ended signals are measured from each signal (true and inverting signals) with respect to ground. The receiver ideally switches at the crossing point of the two signals. LVDS signals have a V_{OD} specification of 250mV to 450mV with a typical V_{OS} of 1.2V. Our devices have a typical V_{OD} of 300mV, but for the example below, we will use a signal between 1.0 V (V_{OL}) and 1.4 V (V_{OH}) for a 400 mV V_{OD}. The differential waveform is constructed by subtracting the Jx-1 (inverting) signal from the Jx-3 (true) signal. V_{OD} = (Jx-3) – (Jx-1). The V_{OD} magnitude is either positive or negative, so the differential swing (V_{SS}) is twice the V_{OD} magnitude. Drawn single-ended waveforms and the corresponding differential waveforms are shown in the following figure.



Single-Ended & Differential Waveforms

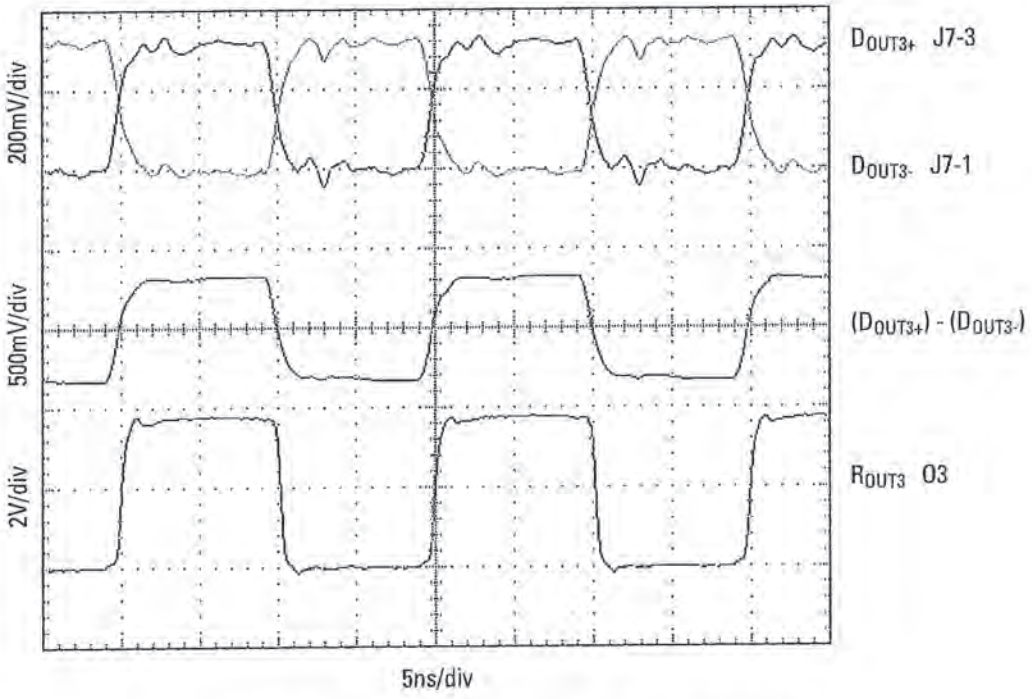
The PCB interconnect signal (LVDS Channel #2) can be measured at the receiver inputs (test points J6-1 and J6-3). Due to the short interconnect path via the PCB little distortion to the waveform is caused by the interconnect. See figure below. Note that the data rate is 100Mbps and the differential waveform (V_{DIFF} = D_{OUT2+} - D_{OUT2-}) shows fast transition times with little distortion.

In the next four figures, the top two waveforms are the single-ended outputs (between the driver and receiver), the middle waveform is the calculated differential output signal from the two single-ended signals and the bottom waveform is the output TTL signal from the receiver.

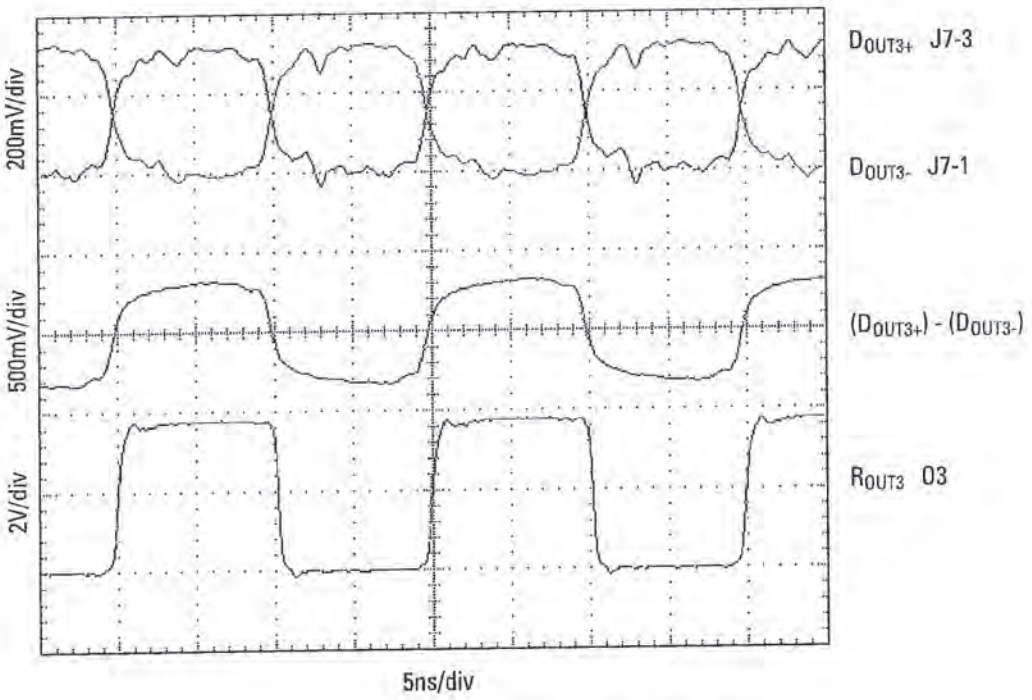


LVDS Channel #2 Waveforms — PCB Interconnect

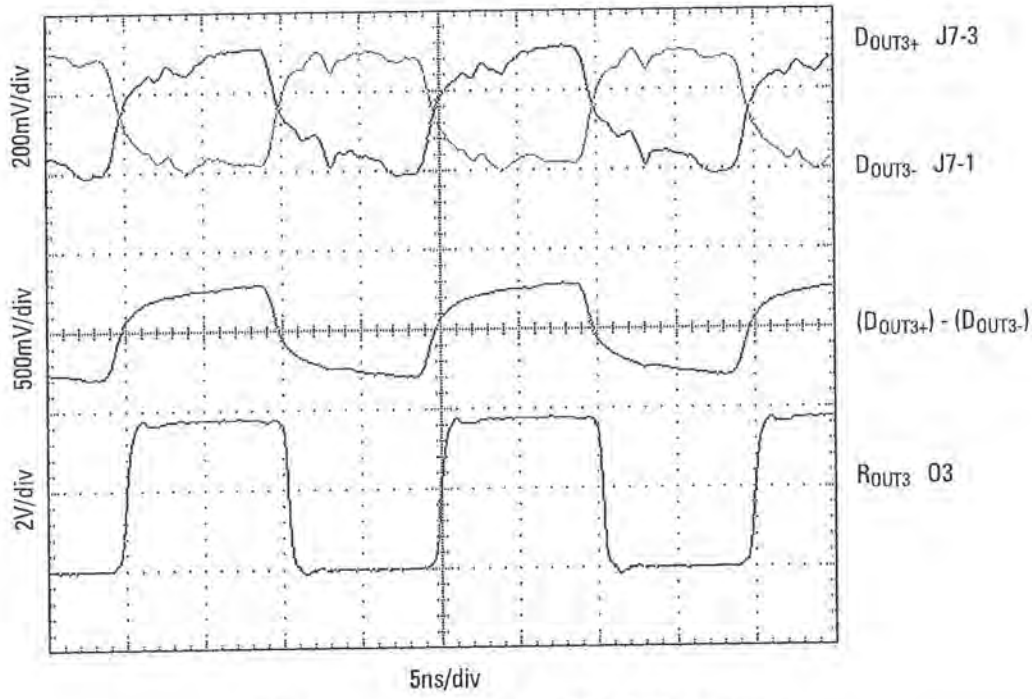
The cable interconnect signal is also measured at the receiver inputs (test points J7-1 & J7-3 and J8-1 & J8-3). Due to the characteristics of the cable some waveform distortion has occurred. Depending upon the cable length and quality, the transition time of the signal at the end of the cable will be slower than the signal at the driver's outputs. This effect can be measured by taking rise and fall measurements and increasing the cable length. A ratio of transition time to unit interval (minimum bit width) is a common gauge of signal quality. Depending upon the application ratios of 30% to 50% are common. These measurements tend to be more conservative than jitter measurements. The waveforms acquired with an RJ45 cable of 1 meter, 5 meters and 10 meters in length are shown in the next three figures. Note the additional transition time slowing due to the cable's filter effects on the 5 meter and 10 meter test case.



LVDS Channel #3 Waveforms - 1m Cable Interconnect



LVDS Channel #3 Waveforms - 5m Cable Interconnect



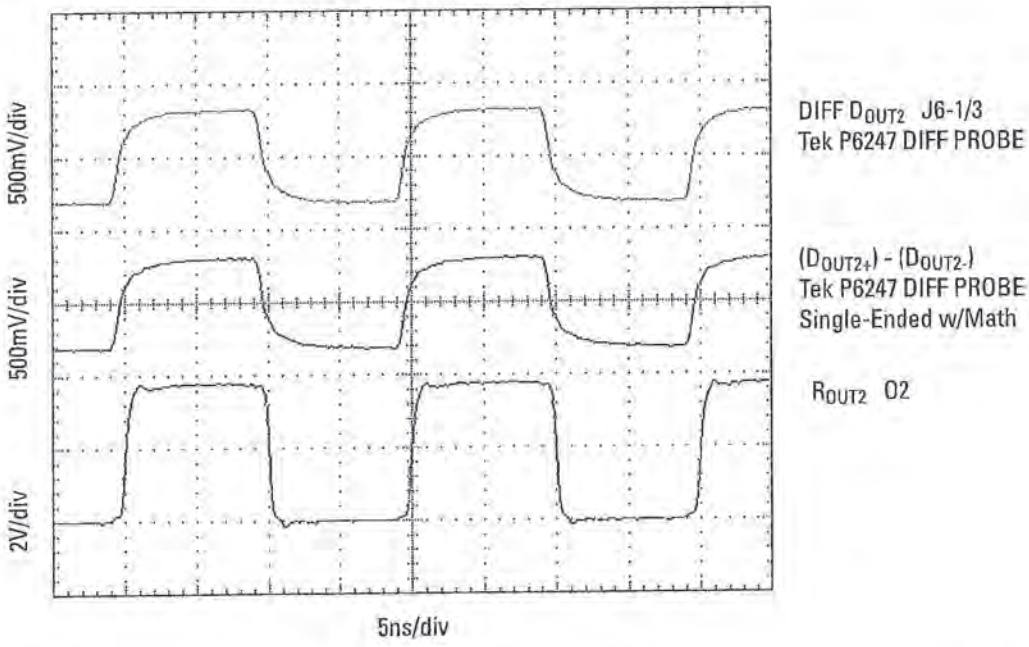
LVDS Channel #3 Waveforms - 10m Cable Interconnect

7.2.7 Probing of High-Speed LVDS Signals

Probe specifications for measuring LVDS signals are unique due to the low drive level of LVDS (3 mA typical). Either a high impedance probe (100kΩ or greater) or the TEK P6247 differential probe (>1GHz bandwidth) must be used. The capacitive loading of the probe should be kept in the low pF range, and the bandwidth of the probe should be at least 1 GHz (4 GHz preferred) to accurately acquire the waveform under measurement.

National's Interface Applications group employs a wide range of probes and oscilloscopes. One system that meets the requirements of LVDS particularly well is a TEK TDS 684B Digital Real Time scope (>1GHz bandwidth) and TEK P6247 differential probe heads. These probes offer 200kΩ, 1pF loading and a bandwidth of 1GHz. This test equipment was used to acquire the waveforms shown.

The TEK P6247 differential probes may be used to measure the differential LVDS signal or each signal of the differential pair single-ended. This test equipment was used to acquire the waveforms differentially as well as single-endedly with the differential signal calculated by (DOUT+) – (DOUT-) shown in the figure below. You can see that both of the differential signals look identical. The method in which you acquire the single-ended signals is important (such as matching probe types and lengths) if you intend to calculate the differential signal from the two single-ended signals.



LVDS Channel #2 Waveforms - Differential and Calculated Differential from Single-Ended Waveform

LVDS waveforms may also be measured with high impedance probes such as common SD14 probe heads. These probes offer 100kΩ, 0.4pF loading and a bandwidth of 4 GHz. These probes connect to a TEK 11801B scope (50 GHz bandwidth). Probes with standard 50Ω loading should not be used on LVDS lines since they will load them too heavily. 50Ω probes may be used on the receiver output signal in conjunction with the 453Ω series resistor option (see option section below). Note that the scope waveform is an attenuated signal (50Ω/(450Ω + 50Ω) or 1/10) of the output signal and the receiver output is loaded with 500Ω to ground.

7.2.8 Demo PCB Options

Option 1: 453Ω Resistors
A provision for a series 453Ω resistor (RS1, RS2, RS3 and RS4) is provided on the receiver output signal. By cutting the trace between the "RS" pads and installing a 453Ω resistor, a standard 50Ω scope probe may be used (500Ω total load). Note that the signal is divided down (1/10) at the scope input.

Option 2: Disabling the LVDS Driver
The quad driver features a ganged enable. An active high or an active low input are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J3). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the driver, connect the jumper to the power plane, to disable the driver connect the jumper to the ground.

Option 3: Disabling the LVDS Receiver
The quad receiver features a ganged enable (same as the driver). An active high or an active low are provided. On the evaluation PCB, the active low input (EN*) is routed to ground. The active high input (EN) is routed to a jumper (J4). The jumper provides a connection to the V_{CC} plane ("ON") or to the Ground plane ("OFF"). To enable the receiver, connect the jumper to the power plane, to disable the receiver connect the jumper to ground.

Option 4: Cables
Different cables may also be tested (different lengths, materials, constructions). A standard RJ45 8-pin connector/pinout has been used (J1 and J2). Simply plug in the RJ45 1 meter or 5 meter cables included in the kit or build a custom cable.

Option 5: SMA or SMB Connectors
Both SMA and SMB connectors will fit the footprint on the boards for the driver inputs I1-4, receiver outputs O1-4 and the single receiver inputs I5-6. The board is loaded with SMBs on I4 and O4.

Option 6: Receiver Termination (Channel #1B)
The separate receiver input signals can be terminated separately (50Ω on each line to ground) utilizing pads RT5 (inverting to ground) and RT6 (true input to ground) for a signal generator interface. In addition, a single 100Ω differential resistor (across pads RT5 and RT6) can be used if the device is to be driven by a differential driver. Be sure to remove the 50Ω termination resistors RT5 and RT6 if you plan to use the 100Ω differential resistor.

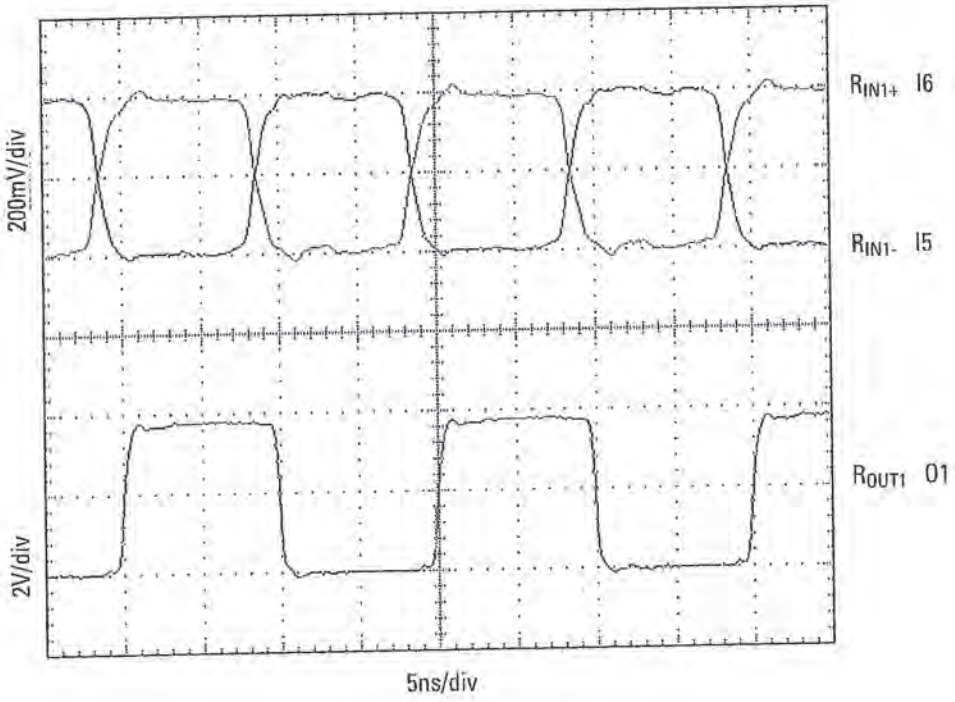
7.2.9 Plug & Play

The following simple steps should be taken to begin testing on your completed evaluation board:

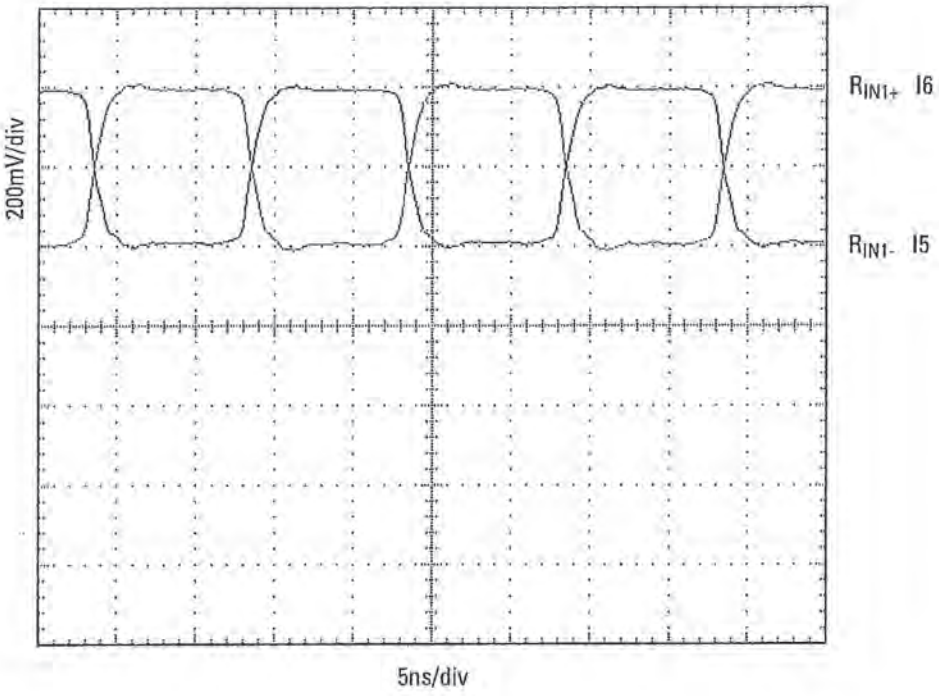
1. Connect signal common (Ground) to the pierced lug terminal marked GND
2. Connect the power supply lead to the pierced lug terminal marked V_{CC} (3.3V)
3. Set J3 & J4 jumpers to the power plane ("ON") to enable the drivers and receivers
4. Connect enclosed RJ45 cable between connectors J1 and J2
5. Connect a signal generator to the driver input (I4) with:
   a) frequency = 50 MHz (100 Mbps)
   b) V_{IL} = 0V & V_{IH} = 3.0V
   c) t_r & t_f = 2 ns
   d) duty cycle = 50% (square wave)
6. Connect differential probes to test points J8-1 and J8-3
7. View LVDS signals using the same voltage offset and volts/div settings on the scope with the TEK P6247 differential probes. View the output signal on a separate channel from test point O4. The signals that you will see should resemble the LVDS Channel #3 Waveform - 1m or 5m Cable Interconnect figure.

7.2.10 Common-Mode Noise

When the receiver (DS90LV048A) is enabled, a small amount of common-mode noise is passed from the output of the receiver to the inputs as shown in the next figure. This noise shows up on the single-ended waveforms, but does not impact the differential waveform that carries the data. A design improvement was made to the DS90LV048A to reduce the magnitude of the noise coupled back to the inputs, reducing the feedback by 30% compared to prior devices. This noise will not be observed if the receiver device is disabled by setting J4 to "OFF" as shown in the following figure.



LVDS Channel #1B Waveforms
A Small Amount of Common-Mode Noise Coupled from Output to Input



LVDS Channel #1B Waveforms – Output Disabled

7.2.11 Summary

This evaluation PCB provides a simple tool to evaluate LVDS signaling across different media and lengths to determine signal quality for high-speed data transmission applications.

7.2.12 Appendix

Typical test equipment used for LVDS measurements:

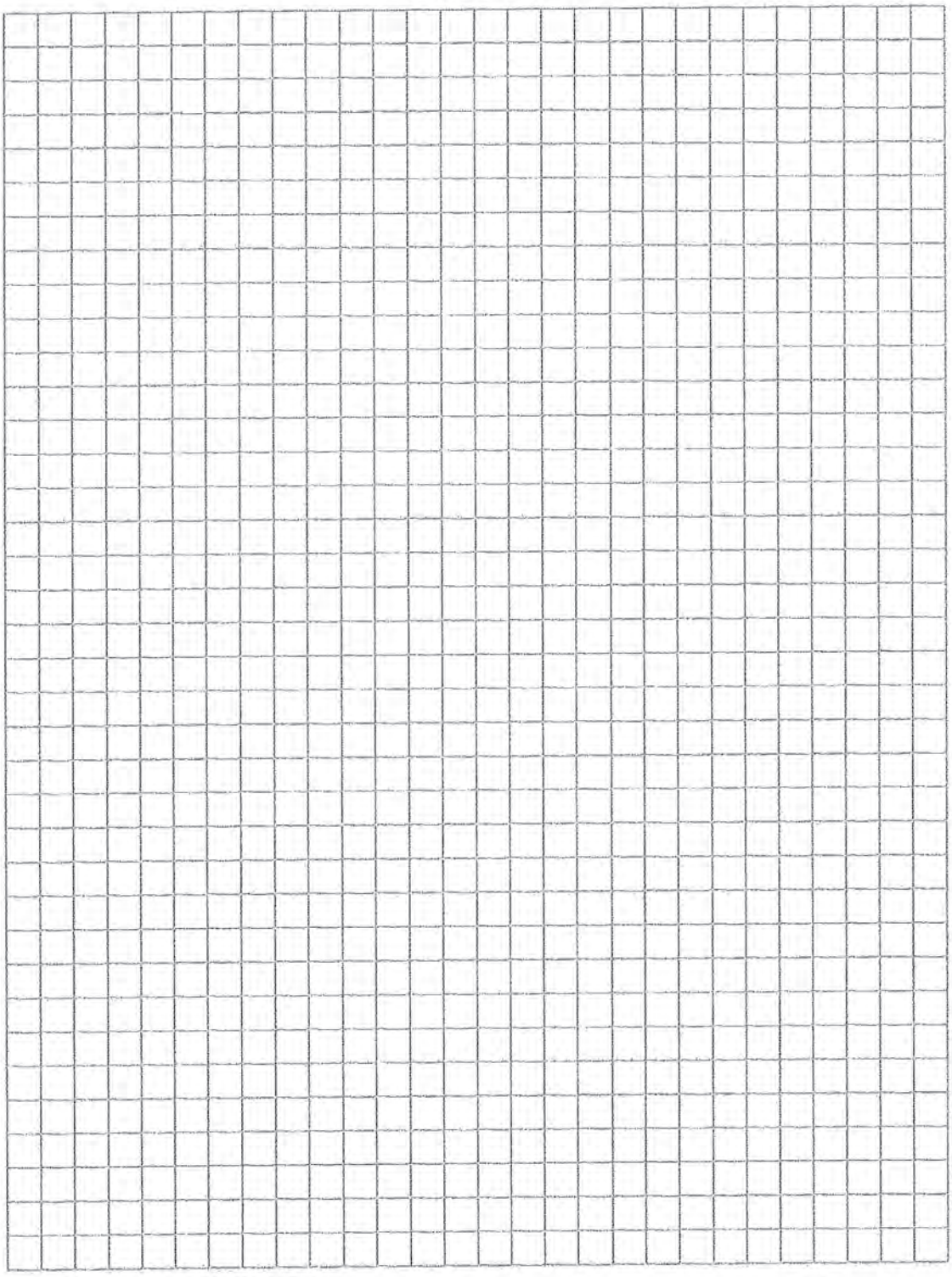
Signal Generator	TEK HFS 9009
Oscilloscope	TEK TDS 684B Digital Real Time scope, TEK 11801B scope
Probes	TEK P6247 differential probe, TEK SD-14 probe

Bill of Materials

Type	Label	Value/Tolerance	Qty	Footprint	Part Number
IC	U1	(Quad Driver)	1	16-L TSSOP	DS90LV047ATMTC
IC	U2	(Quad Receiver)	1	16-L TSSOP	DS90LV048ATMTC
Connector	J1, J2	(8-pin RJ45)	2		AMP P/N 558310-1
Resistor	RT1-6	50Ω	6	RC0805	
Resistor	RL1-4	100Ω	4	RC0805	
Resistor	RS1, RS2, RS3, RS4	453Ω	0/4	RC0805	not loaded
Capacitor	CB1, CB2, CB3	0.1µF	3	CC0805	
Capacitor	CB13	0.01µF	1	CC0805	
Capacitor	CB21, CB22, CB23	0.001µF	3	CC0805	
Capacitor	CBR1	10µF, 35V	1	D	Solid Tantalum Chip Capacitor
Headers	J3, J4	3 lead header	2		100 mil spacing (single row header)
Headers	J5, J6, J7, J8	4 lead header	4		100 mil spacing (double row header)
Jumpers		0.1 jumper post shunts	2		
SMB Jack	I4, O4		2	SMB Connector	Johnson P/N 131-3701-201
*SMB Jack or *SMA Jack	I1-3, I5-6, O1-3		0/8	SMB Connector SMA Connector	Johnson P/N 131-3701-201 Johnson P/N 142-0701-201
Plug (banana)	V_{CC}, GND	Uninsulated Standard Pierced Lug Terminal	2		Johnson P/N 108-0740-001
Cable		RJ45 Cable	2		1 meter and 5 meter
Legs			4		
Bolts/washers			4		
PCB			1		LVDS47/48PCB

* Note: On the evaluation board, inputs I1-3, I5-6 and outputs O1-3 are not loaded with connectors. These inputs and outputs can be loaded with either SMBs (P/N 131-3701-201) or SMAs (P/N 142-0701-201).

NOTES



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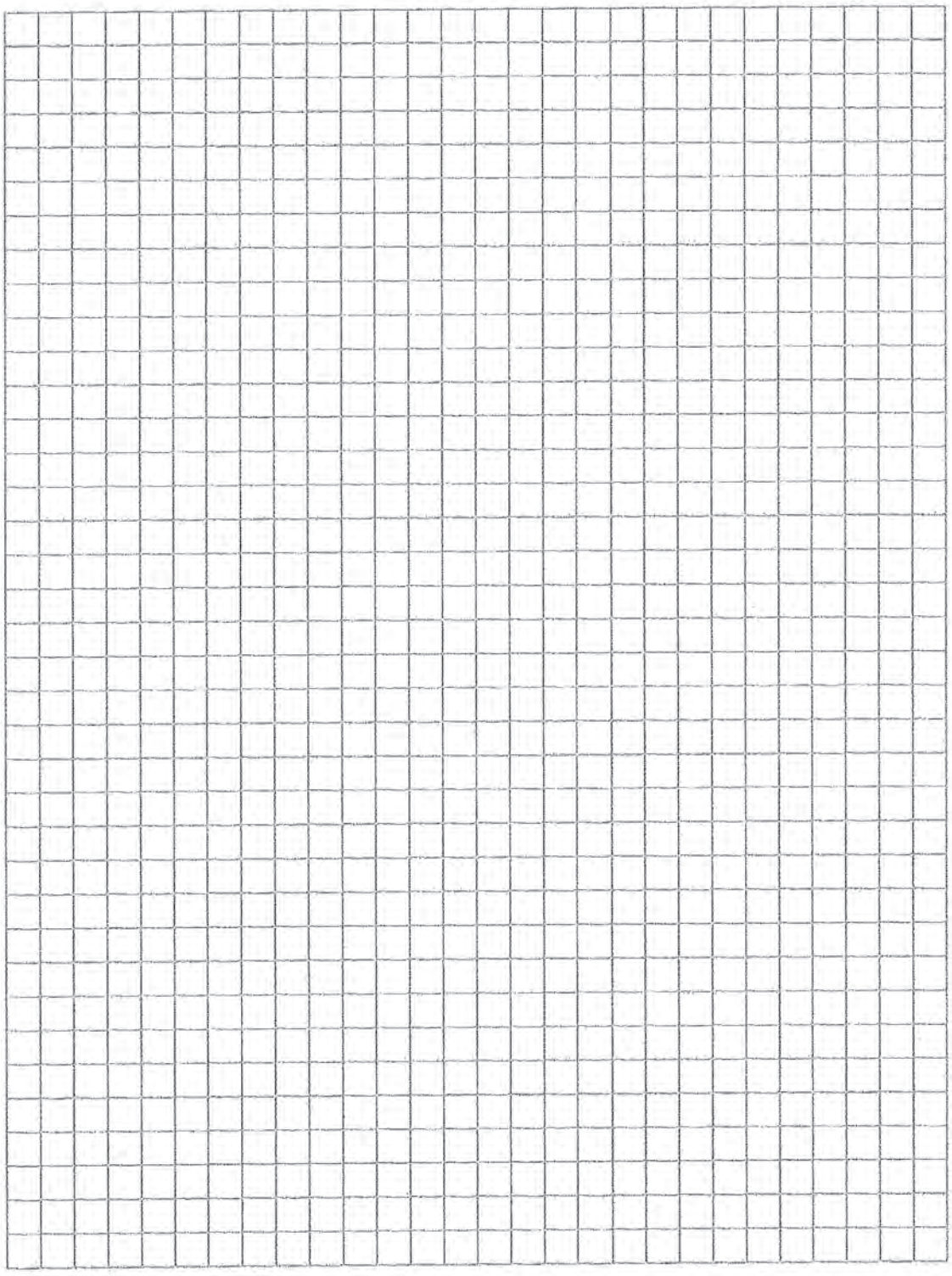


LVDS Reference

Chapter 8

8.0.0 LVDS REFERENCE – APPLICATION NOTES, STANDARDS, WHITE PAPERS, MODELING INFORMATION AND OTHER DESIGN GUIDES

8.1.0 NATIONAL DOCUMENTS

National also offers more in depth application material on LVDS in the form of application notes, conference papers, white papers and other documents. Please visit the LVDS website for the viewing or downloading of documents. The website's URL is: **www.national.com/appinfo/lvds/**

8.1.1 National LVDS Application Notes

The following application notes on LVDS are currently available:

AN-Number	Topic	Parts Referenced
AN-971	Introduction to LVDS	DS90C031/DS90C032
AN-977	Signal Quality – Eye Patterns	DS90C031
AN-1040	Bit Error Rate Testing	DS90C031/DS90C032
AN-1041	Introduction to Channel Link	DS90CR2xx
AN-1059	Timing (RSKM) Information	DS90CRxxx
AN-1060	LVDS - Megabits @ milliwatts (EDN Reprint)	
AN-1084	Parallel Application of Link Chips	DS90Cxxx
AN-1088	Bus LVDS/LVDS Signal Quality	DS90LV017/27, DS92LV010A
AN-1108	PCB and Interconnect Design Guidelines	DS90CR2xx
AN-1109	Multidrop Application of Channel Links	DS90CR2xx
AN-1110	Power Dissipation of LVDS Drivers and Receivers	DS90C031/2, DS90LV031A/32A
AN-1115	Bus LVDS and DS92LV010A XCVR	DS92LV010A
AN-1123	Sorting Out Backplane Driver Alphabet Soup	

8.1.2 National Application Notes on Generic Data Transmission Topics

National also offers many application notes devoted to the general topics of data transmission, PCB design and other topics pertaining to Interface. A few of these are highlighted below.

AN-Number	Topic
AN-216	An Overview of Selected Industry Interface Standards
AN-643	EMI/RFI Board Design
AN-806	Data Transmission Lines and Their Characteristics
AN-807	Reflections: Computations and Waveforms
AN-808	Long Transmission Lines and Data Signal Quality
AN-912	Common Data Transmission Parameters and their Definitions
AN-916	A Practical Guide to Cable Selection
AN-972	Inter-Operation of Interface Standards
AN-1111	An Introduction to IBIS Modeling

A complete list of all application notes is located at: **http:www.national.com/apnotes/apnotes_all_1.html**

8.1.3 National Application Notes on Flat Panel Display Link/LVDS Display Interface

A series of application notes is available on the FPD-Link and LDI chipsets. Please see the FPD website for a list of application notes that are currently available at:

www.national.com/appinfo/fpd/

8.1.4 Conference Papers/White Papers from National

The following conference papers are currently available from the LVDS website at:

www.national.com/appinfo/lvds/

- **BLVDS White Paper**
  Signal Integrity and Validation of Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes.
  DesignCon99 Paper
- **BLVDS White Paper**
  A Baker's Dozen of High-Speed Differential Backplane Design Tips.
  DesignCon2000 Paper
- **BLVDS White Paper**
  Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS).
  DesignCon2000 Paper

8.1.5 Design Tools - RAPIDESIGNERS

The National Semiconductor Transmission Line RAPIDESIGNERs make quick work of calculations frequently used in the design of data transmission line systems on printed circuit boards. Based on principles contained in the National Interface Databook, the Transmission Line RAPIDESIGNER benefits from our many years of experience in designing and manufacturing data transmission and interface products and from helping our valued customers obtain the most from National's Interface Products.

The following calculations can be made with the RAPIDESIGNER for both Microstrip and Stripline geometries.

- Characteristic Impedance (Z_O)
- Intrinsic Delay
- Unterminated Stub Length
- Loaded Impedance
- Differential Impedance
- Propagation Delay
- Reflection Coefficient
- C_O and L_O
- Reactance Frequency

Two versions of the popular RAPIDESIGNER are available while supplies last. The two RAPIDESIGNERs differ in the dimensions supported; one is for METRIC units while the other supports ENGLISH units.

- RAPIDESIGNER, Metric Units, LIT# 633200-001
- RAPIDESIGNER, English Units, LIT# 633201-001

A full Operation and Application Guide is provided in AN-905. Also included in the application note are the formulas for the calculations, accuracy information, example calculations and other useful information.

To obtain a RAPIDESIGNER, contact the National Customer Support Center in your area.

8.2.0 LVDS STANDARD – ANSI/TIA/EIA-644

Copies of the ANSI/TIA/EIA-644 LVDS Standard can be purchased from Global Engineering Documents. Contact information that was current at the time this book was printed is:

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112-5704

or call

USA and Canada: 1.800.854.7179
International: 1.303.397.7956

http://global.ihs.com/

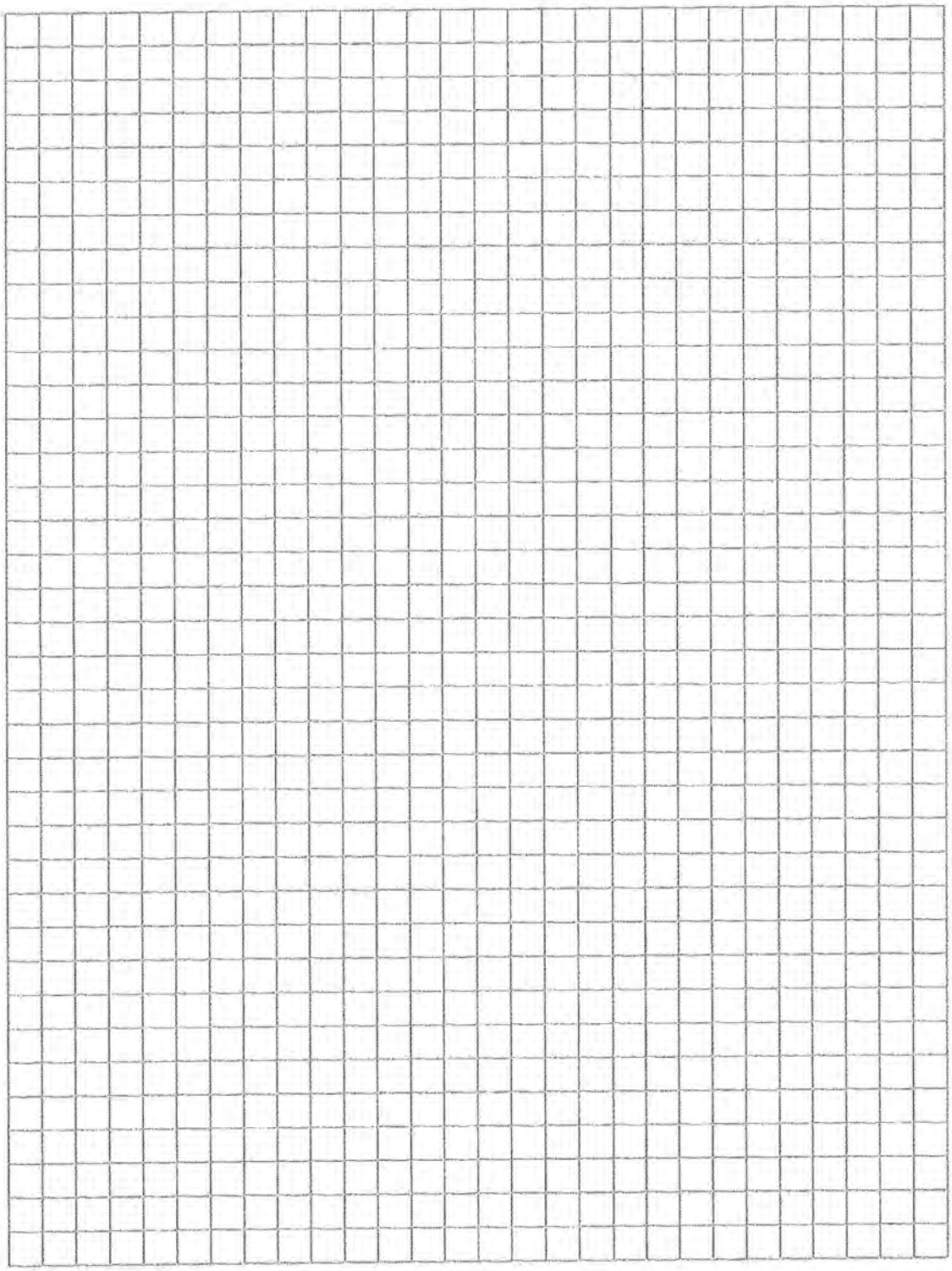
8.3.0 IBIS I/O MODEL INFORMATION

I/O Buffer Information Specification (IBIS) is a behavioral model specification defined within the ANSI/EIA-656 standard. LVDS IBIS models are available from National's Website which can be used by most simulators/EDA tools in the industry. Please see: http:www.national.com/models/ibis/Interface/

Also, visit the ANSI/EIA-656 Website: www.eia.org/EIG/IBIS/ibis.htm for a vendor listing or contact your software vendor.

Chapter 13 of National's 1999 Interface Databook (LIT# 400058) describes IBIS models in detail. A major portion of this material is also covered in National's Application Note AN-1111.

NOTES



National's LVDS Website

Chapter 9

9.0.0 LVDS WEBSITE CONTENTS

9.1.0 NATIONAL WEBSITE

National provides an extensive website targeted for Design Engineers and also Purchasing/Component Engineers. From the main page, you can find:

- Product Tree/Selection Guide
- Datasheets
- Application Notes
- Product Folders
  - View/Download: General Descriptions, Features or the Entire Datasheet
  - Product Status and Pricing Information
  - Application Note Reference
- Packaging Information
- Marking Information
- Technical Support
- Search Engine
- Databooks, CD ROMs and Samples

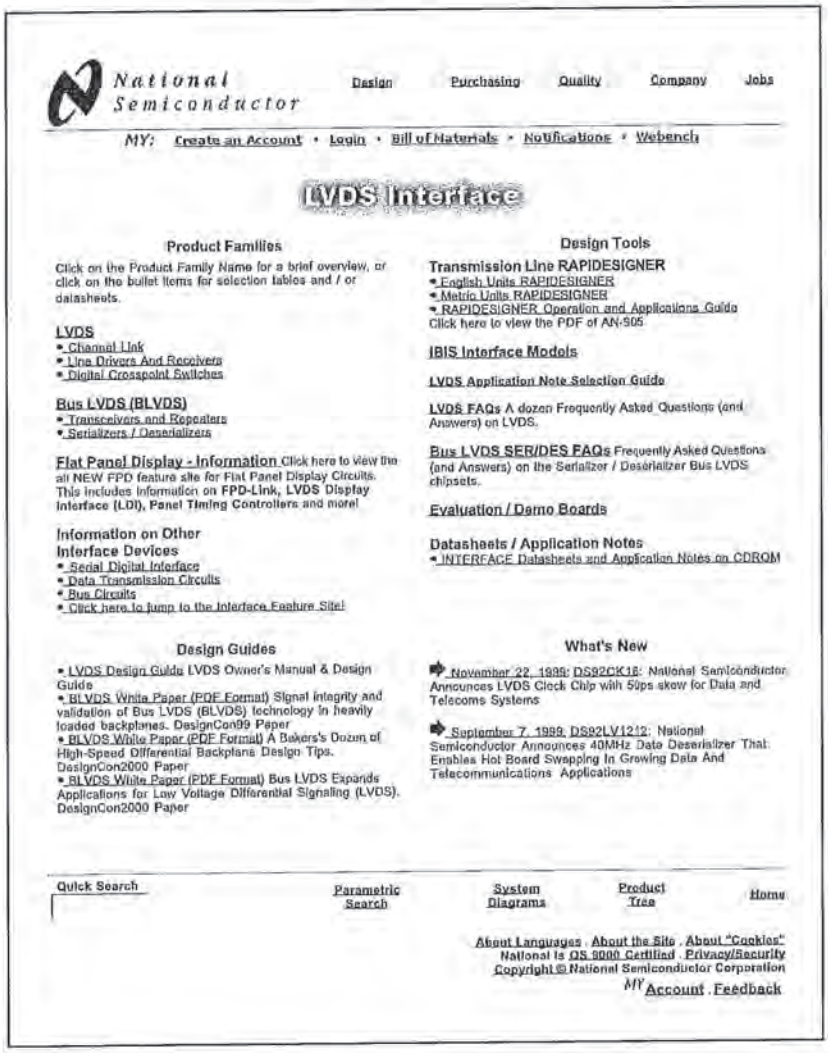
The website's URL is: www.national.com

9.2.0 NATIONAL'S LVDS APPINFO WEBSITE

National provides an in depth application site on LVDS. This site provides the design community with the latest information on National's expanding LVDS family. Please visit the LVDS website to view or download documents. On this site, you can locate:

- LVDS Selection Tables
- Frequently Asked Questions (and Answers)
- Application Note Cross Reference Table (AN Number – Topic – Device ID)
- Interface IBIS Models
- Evaluation Boards – Documentation and Ordering Information
- Family Introductions/Overviews
- Design Tools – RAPIDESIGNERS
- Press Releases

The website's URL is: www.national.com/appinfo/lvds/



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LVDS Interface

Product Families

Click on the Product Family Name for a brief overview, or click on the bullet items for selection tables and / or datasheets.

LVDS
- Channel Link
- Line Drivers And Receivers
- Digital Crosspoint Switches

Bus LVDS (BLVDS)
- Transceivers and Repeaters
- Serializers / Deserializers

Flat Panel Display - Information Click here to view the all NEW FPD feature site for Flat Panel Display Circuits. This includes information on FPD-Link, LVDS Display Interface (LDI), Panel Timing Controllers and more!

Information on Other Interface Devices
- Serial Digital Interface
- Data Transmission Circuits
- Bus Circuits
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Design Tools

Transmission Line RAPIDESIGNER
- English Units RAPIDESIGNER
- Metric Units RAPIDESIGNER
- RAPIDESIGNER Operation and Applications Guide

Click here to view the PDF of AN-905

IBIS Interface Models

LVDS Application Note Selection Guide

LVDS FAQs A dozen Frequently Asked Questions (and Answers) on LVDS.

Bus LVDS SER/DES FAQs Frequently Asked Questions (and Answers) on the Serializer / Deserializer Bus LVDS chipsets.

Evaluation / Demo Boards

Datasheets / Application Notes
- INTERFACE Datasheets and Application Notes on CDROM

Design Guides
- LVDS Design Guide LVDS Owner's Manual & Design Guide
- BLVDS White Paper (PDF Format) Signal integrity and validation of Bus LVDS (BLVDS) technology in heavily loaded backplanes. DesignCon99 Paper
- BLVDS White Paper (PDF Format) A Baker's Dozen of High-Speed Differential Backplane Design Tips. DesignCon2000 Paper
- BLVDS White Paper (PDF Format) Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS). DesignCon2000 Paper

What's New

November 22, 1999: DS92CK16: National Semiconductor Announces LVDS Clock Chip with 50ps skew for Data and Telecoms Systems

September 7, 1999: DS92LV1212: National Semiconductor Announces 40MHz Data Deserializer That Enables Hot Board Swapping In Growing Data And Telecommunications Applications

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Screen shot of LVDS APPINFO website: www.national.com/appinfo/lvds/

9.3.0 OTHER NATIONAL'S APPINFO WEBSITES

9.3.1 "INTERFACE" Products

National provides an application site on INTERFACE. This site provides the design community with the latest information on National's expanding SDI (Serial Digital Interface) and RS-xxx families. Please visit the INTERFACE website to view or download documents.

9.3.2 "FPD" Products

National provides an in depth application site on Flat Panel Display devices. This site provides the design community the latest information on National's expanding FPD-Link, LDI and TCON families. Please visit the FPD website to view or download documents.

9.3.3 Other/APPINFO/Websites

National provides other in depth application sites. Please visit the main-page for an updated list of pages. This site can be viewed at: **http:www.national.com/appinfo**. It currently includes information on:

- A/D Converters
- Advanced I/O
- Amplifiers
- Audio Products
- Automotive
- Compact RISC
- Custom
- Die Products
- Enhanced Solutions
- Flat Panel Display
- Information Appliance Solutions
- Interface
- LTCC Foundry
- LVDS Interface Products
- Microcontroller
- Micro SMD
- Power
- Scanners
- Temperature Sensors
- USB Technologies
- Wireless Products
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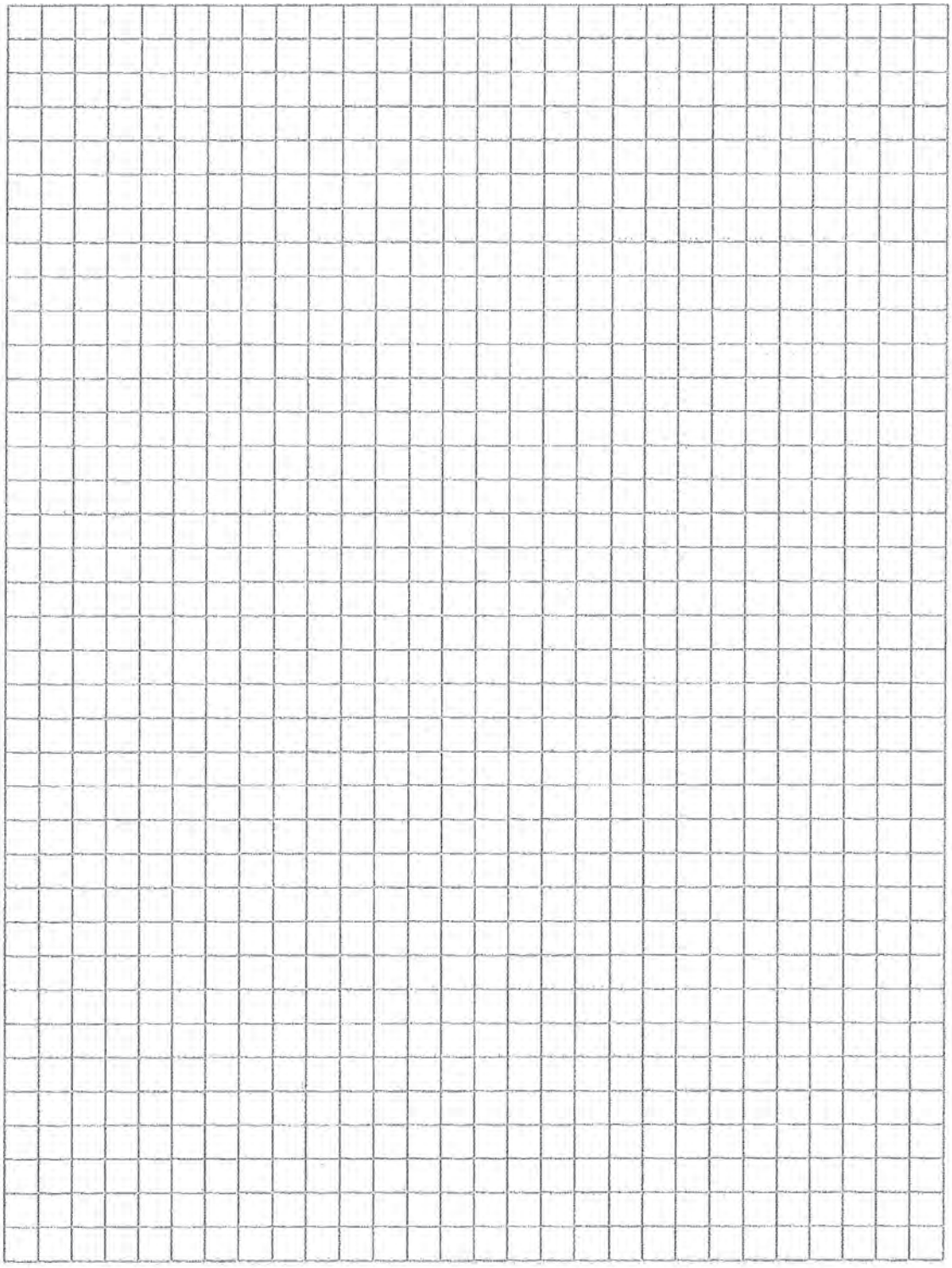

Glossary, Index and Worldwide Sales Offices

Appendix

GLOSSARY

AN	Application Note
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
B/P	Backplane
BER	Bit Error Rate
BERT	Bit Error Rate Test
BLVDS	Bus LVDS
BTL	Backplane Transceiver Logic
CAT3	Category 3 (Cable classification)
CAT5	Category 5 (Cable classification)
CISPR	International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques)
D	Driver
DCR	DC Resistance
DUT	Device Under Test
ECL	Emitter Coupled Logic
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharge
EVK	Evaluation Kit
FCC	Federal Communications Commission
FPD	Flat Panel Display
FPD-LINK	Flat Panel Display Link
Gbps	Gigabits per second
GTL	Gunning Transceiver Logic
Hi-Z	High Impedance
IC	Integrated Circuit
I/O	Input/Output
IBIS	I/O Buffer Information Specification
IDC	Insulation Displacement Connector
IEEE	Institute of Electrical and Electronics Engineers
kbps	kilobits per second
LAN	Local Area Network

GLOSSARY (continued)

LDI	LVDS Display Interface
LVDS	Low Voltage Differential Signaling
Mbps	Mega bits per second
MDR	Mini Delta Ribbon
MLC	Multi Layer Ceramic
NRZ	Non Return to Zero
PCB	Printed Circuit Board
PECL	Pseudo Emitter Coupled Logic
PHY	Physical layer device
PLL	Phase Lock Loop
PRBS	Pseudo Random Bit Sequence
R	Receiver
RFI	Radio Frequency Interference
RS	Recommended Standard
RT	Termination Resistor
RX	Receiver
SCI	Scalable Coherent Interface
SCSI	Small Computer Systems Interface
SDI	Serial Digital Interface
SER/DES	Serializer/Deserializer
SUT	System Under Test
T	Transceiver
TDR	Time Domain Refletometry
TEM	Transverse Electro-Magnetic
TFT	Thin Film Transistor
TI	Totally Irrelevant
TIA	Telecommunications Industry Association
TP	Test Point
TTL	Transistor Transistor Logic
TWP	Twisted Pair
TX	Transmitter
UTP	Unshielded Twisted Pair
VCM	Voltage Common-mode
VCR	Video Cassette Recorder

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APPENDIX F

An Overview of LVDS Technology

National Semiconductor
Application Note 971
Syed B. Huq
John Goldie
July 1998

INTRODUCTION

Recent growth in high-end processors, multi-media, virtual reality and networking has demanded more bandwidth than ever before. But the point-to-point physical layer interfaces have not been able to deal with moving information at the data rates required. Some of today's biggest challenges that remain to be solved include: the ability to transfer data fast, lower power systems than currently available, and economical solutions to overcome the physical layer bottleneck. Data Transmission standards like RS-422, RS-485, SCSI and others all have their own limitations most notably in transferring raw data across a media. Not anymore. Low Voltage Differential Signaling (LVDS) is a high speed (>155.5 Mbps), low power general purpose interface standard that solves the bottleneck problems while servicing a wide range of application areas.

This application note explains the key advantages and benefits of LVDS technology. Throughout this application note the DS90C031 (LVDS 5V Quad CMOS Differential Line Driver) and the DS90C032 (LVDS 5V Quad CMOS Differential Line Receiver) will be used to illustrate the key points. Over 50 LVDS devices are offered currently (1998) from National, please refer to the LVDS device datasheets for complete specifications.

STANDARDS OVERVIEW

There are two industry standards that define LVDS. The more common of the two is the generic electrical layer standard defined by the TIA. This standard is know as ANSI/TIA/EIA-644. The other application specific standard is an IEEE (Institute for Electrical and Electronics Engineering) standard titled Scalable Coherent Interface (SCI).

ANSI/TIA/EIA-644

This standard was developed under the Data Transmission Interface committee TR30.2. This standard defines driver output and receiver input characteristics. Functional specifications and/or Protocols are not within the scope of the TIA standard. It notes a recommended maximum data rate of 655 Mbps and a theoretical maximum of 1.923 Gbps based on a loss-less media; however, maximum data rate is application (desired signal quality), and device specific (transition time). It is feasible that LVDS based interface will operate in the 500 Mbps to 1.5Gbps range in the near future. Minimum media specifications are also defined within the standard. It also discusses failsafe operation of the receiver under fault conditions and other configurations issues such as multi-receiver operation. National Semiconductor held the editor position for this standard.

IEEE 1596.3 SCI-LVDS

SCI originally referenced a differential ECL interface within the SCI (Scalable Coherent Interface) 1596-1992 IEEE standard. But, this only addressed the high data rates required and did not address the low power concerns. Thus, SCI-LVDS was defined as a subset of SCI, and is specified in IEEE 1596.3 standard. SCI-LVDS specifies signaling levels (electrical specifications) for the high speed/low power physical layer interface. It also defines the encoding for packet switching used in SCI data transfers. Packets are constructed from 2-byte (doublet) symbols. This is the fundamental 16-bit symbol size. No media is specified and the data rate can be in the order of 500 MT/s based on serial or parallel transmission of 1, 4, 8, 16, 32, 64,.... bits.

SCI-LVDS also supports RamLink for super low power data transmission in a restricted environment. The IEEE 1596.3 standard was approved in March 1994. National Semiconductor held the Chairperson position for this standard.

SCI-LVDS is similar to the TIA version but differs in some electrical requirements and load conditions. Both standards feature similar driver output levels, receiver thresholds and data rates. The TIA version is the more generic of the two standards and is intended for multiple applications.

LOW VOLTAGE DIFFERENTIAL SIGNALING

LVDS technology uses differential data transmission. The differential scheme has a tremendous advantage over single-ended schemes as it is less susceptible to common mode noise. Noise coupled onto the interconnect is seen as common mode modulations by the receivers and is rejected. The receivers respond only to differential voltages.

LVDS technology is not dependent on a specific power supply, such as +5V. This means there is an easy migration path to lower supply voltages such as +3.3V, +2.5V or even lower while still maintaining the same signaling levels and performance. Technologies like ECL or PECL are more dependent on the supply voltage. This feature is highly desirable in any application that foresees moving to lower supply voltages without substantial redesign or worrying about mixed voltage operation (+5V/+3.3V) on system boards.

To achieve high data rate, low power and to reduce EMI effects, signaling levels have to be reduced. The DS90C031/DS90C032 chipset's limitation on data rate is mainly dependent on the technology driving the LVDS drivers. The aggregate bandwidth that LVDS technology can drive is in the Gbps range with a loss-less media. Data rates in the 500-1,000 Mbps are possible and this limitation is primarily dependent on the media being driven.

SIGNALING LEVELS

As the name implies, LVDS features a **low voltage** swing compared to other industry data transmission standards. The signaling levels are illustrated in *Figure 1*, and a comparison to PECL levels is also shown as reference. Because of the low swing advantage, LVDS achieves a high aggregate bandwidth in point-to-point applications. National has recently introduced a new family of parts called Bus LVDS. This family extends LVDS from point-to-point applications to multi-point applications is fully discussed in other National application notes. Bus LVDS features similar voltage swings, but provides increased drive current to handle double terminations required in multi-point applications.

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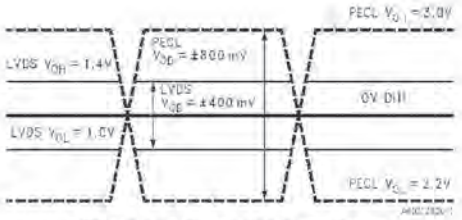

FIGURE 1. PECL vs LVDS Signal Swing

It is impossible to achieve high data rates and provide low power without utilizing low voltage swings. LVDS signaling levels are smaller (50%) than PECL levels as shown in *Figure 1*. EMI effects are also reduced as the signaling swings are much smaller than traditional CMOS, TTL or even PECL. This is due to the current mode drivers, the soft transitions, the low switching currents and the use of true differential data transmission.

LVDS TERMINATION

LVDS uses a constant current mode driver to obtain its many features. The value of the current source for the DS90C031 is a maximum of 4.5 mA. The transmission media must be terminated to its characteristic impedance to prevent reflections. Typically this is between 100Ω–120Ω and is matched to the actual cable. *A termination resistor is required* to generate the Differential Output Voltage (V_{OD}) across the resistive termination load at the receiver input (see *Figure 2 A*). Data transmission from the driver to receiver without the termination is not recommended. The simplicity of the LVDS termination scheme makes it easy to implement in most applications. It is recommended to have a single 100Ω1termination between the driver outputs, and the use of surface mount components is also recommended to reduce the effects of parasitics. The single resistor approach is the most common LVDS termination method because of its simplicity. Proper termination not only avoids reflection problems, but also reduces unwanted electromagnetic emissions.

The user may also use a cable damping resistor with a capacitor to ground as shown in *Figure 2B*. This method provides additional common mode termination. Due to the additional complexity, this approach is not too common.

ECL and PECL require more complex terminations than the "one" resistor solution for LVDS. PECL drivers typically require 220Ω pull down resistors from each driver output to ground along with the 100Ω across the driver outputs as shown in *Figure 2C*. This termination method requires additional PCB space and increases system cost compared to the single resistor LVDS termination.

COMMON MODE RANGE

An LVDS receiver can tolerate a minimum of ±1V ground shift between the driver's ground and the receiver's ground. Note that LVDS has a typical driver offset voltage of +1.2V, and the summation of ground shifting, driver offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the receiver is +0.2V to +2.2V, and the recommended receiver input voltage range is from ground to +2.4V. For example, if a driver has a V_{OH} of 1.4V and a V_{OL} of 1.0V (with respect to the driver ground), and a +1V ground shift is present (driver ground +1V higher than receiver ground), this will become +2.4V (1.4+1.0) as V_{IH} and +2.0V (1.0+1.0) as V_{IL} on the receiver inputs referenced to the receiver ground (+2.2V V_{CM}). Similarly, with a −1V ground shift and the same driver levels results as 0.4V (1.4−1.0) V_{IH} and 0.0V (1.0−1.0) V_{IL} on the receiver inputs (+0.2V V_{CM}). This is shown graphically in *Figure 3*.

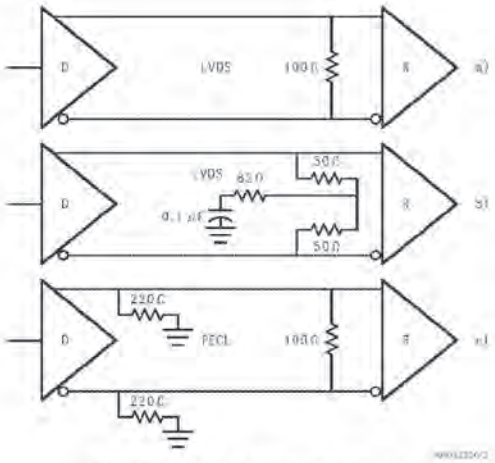

FIGURE 2. a, b, c. Termination Schemes

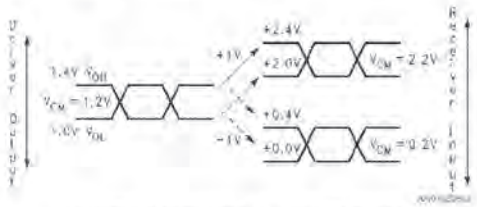

FIGURE 3. Common Mode Voltage Range

FAILSAFE FEATURE

Failsafe is a receiver feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. This occurs when the inputs of the receiver are either open, shorted or terminated.

In some applications, not all receivers of the Quad DS90C032 may be used. In this case, the unused receiver inputs should be left *open*. If the receiver does not support failsafe and the inputs are left *open* (See *Figure 4*), any external noise above the receiver threshold can trigger the output and cause an error on the communication line. Since the DS90C032 supports open input failsafe, the receiver output will provide an output High for this case.

Another fault condition can occur if the inputs get accidentally *shorted* (See *Figure 4*). Under the above condition, the receiver output will also be at logic High and not in an unknown state.

Another case could occur if the driver is either powered off, in TRI-STATE® or even removed from the line while the receiver stays powered on with inputs *terminated* by the 100Ω termination resistor.

The receiver output will provide a logic high under all the above mentioned conditions. Failsafe support is receiver device dependent, please refer to the specific LVDS receiver datasheets to determine which level of failsafe support is provided. Remember that the receiver function is to amplify very small (mV), short duration (ps-ns) pulses to rail-to-rail CMOS levels. System design should ensure that noise picked up on the interconnect is seen as common and not differential. This can be accomplished by using balanced cables, shielding from noise sources and closely-coupled differential traces on PCBs.

POWER ON/OFF REQUIREMENTS and HIGH IMPEDANCE BUS PINS

Depending upon the application high impedance bus pin may or may not be required. This refers to the loading effect of driver outputs and receiver inputs when power is off to the device. First generation LVDS parts were intended for use in point-to-point applications. In this configuration, when the driver is OFF, disabled, or unplugged, the link is down and no communication occurs. The bus loading effects of the device is of minor concern. The DS90C031/DS90C032 family of devices have direct ESD protection pins on the bus pins. Even if a driver is active and a receiver is powered off, the output current is tightly limited and will not cause a latch-up condition to occur on the receiver input.

Second generation devices offered by National (DS90LV031A/DS90LV032A) are intended for a wider range of applications where high impedance bus pins may be required. For this family of devices, the ESD protection circuitry will not load the line when the device is powered off.

To determine if a device supports high impedance bus pins, refer to the features list in the device datasheet and also the

receiver input current parameters and the driver output leakage parameters. National's family of Bus LVDS parts also feature high impedance bus pins as they are intended for multi-drop and multi-point applications.

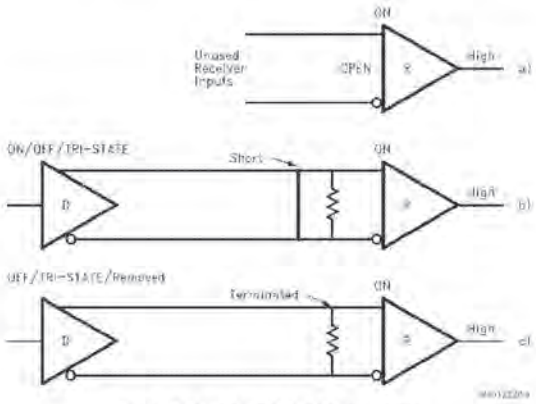

FIGURE 4. a, b, c. Failsafe Operation

POINT-TO-POINT CONFIGURATIONS

For interfaces where the transition time of the driver is substantially shorter than the time delay of the media, the interconnection must be considered a distributed load, not a lumped load. The distributed elements of a transmission line (media) can greatly affect signal quality.

More explicitly, transmission line theory dictates that if the transition (rise or fall) time of the driver is less than four times the line delay, the media must be treated as a distributed load, not a lumped load, and careful attention must be paid to any impedance discontinuities and stubs. For a given driver, if $t_r < 4\ t_d$ (where t_r = driver rise time, t_d = delay of the line) then the line should be considered as a lossy line. This is usually true if the t_r of drivers are in the sub nanosecond range. A quick calculation will clarify this rule of thumb. For example, the DS90C031 driver has a typical t_r of 350 ps, and a microstrip built with FR-4 material has a t_d of 147 ps for one inch of PC trace. This calculates that, an inch of FR-4 microstrip will act as a transmission line (350 < 4*147) when driven by the DS90C031 driver. *Figure 5* includes a stub between the termination resistor and the receiver input. This length must not be longer than one inch in length and should be kept as short as possible. Stub lengths of 1 inch or greater will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Multiple reflections can travel up and down the line causing ringing, overshoot and undershoot which reduces the noise margin too.

The fast t_r of the DS90C031 allows the driver to achieve a higher bandwidth, but transmission line characteristics can easily crop up on a system board if not handled properly at these edge rates. To make the device work to its fullest capability, the LVDS DS90C031 and the DS90C032 should be operated in a point-to-point configuration with minimum discontinuities on the transmission line. This ensures no stub problems on the line. The media ***must*** be terminated by a 100Ω line-to-line termination at the far end. A 100Ω termination resistor terminates the two differential line in its characteristic impedance and also provides the differential voltage (V_{OD}) for the current mode driver. Under the above conditions, the driver can drive a twp (twisted pair) wire over 10m at speeds in excess of 155.5 Mbps (77.7 MHz). Note that other LVDS devices offered by National support higher data rate operation. The FAST LVDS family of parts support 400 Mbps operation, and the Channel Link family of LVDS parts operate even faster on the LVDS lines.

BI-DIRECTIONAL APPLICATION ON ONE TWP

In a bi-directional application data can flow in only one direction at a time (see *Figure 6*) over the single twisted pair, however the bus needs to be terminated at both ends. This requires two 100Ω terminating resistors, assuming the cable impedance is 100Ω (one direction at a time). In *Figure 6*, Rt1 terminates the signal when D1 is driving, and Rt2 terminates the signal when D2 is driving. But, since the drivers are current mode (~4 mA) devices, the two resistors in parallel will load down the driver (100Ω | 100Ω = 50Ω) which cuts the signal in half. This reduces system noise margin to only 25 mV, as the minimum driver V_{OD} is now 125 mV, and the receiver threshold is 100 mV.

Since the driver output swing is severely attenuated due to dual parallel termination load, the bi-directional approach over one twp is not recommended with standard LVDS devices. Bus LVDS devices are recommended for use in applications that employ two terminations (see AN-1115).

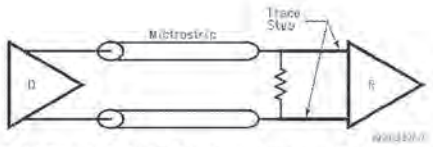

FIGURE 5. A Point-to-Point Configuration Using LVDS

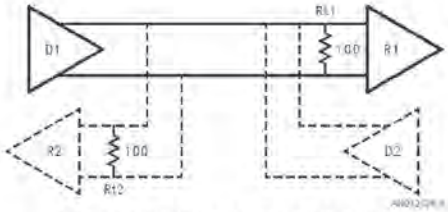

FIGURE 6. Bi-Directional Application over One Pair of Twp

MULTI-DROP CONFIGURATION

In a multi-drop configuration (see *Figure 7*), 10 receivers or more can be tied to the bus. Select an LVDS receiver that supports high impedance bus pins, if the devices use separate power supplies and some receivers may be powered off while communication is flowing from the driver to other powered up receivers. Also, the stubs between the line and each receiver have the potential to create reflections if they are too long, or cause an impedance discontinuity. Remember that only one termination resistor should be used and it must be located at the far end of the cable.

SIGNAL QUALITY ACROSS CABLE

There are numerous ways of determining signal quality on the transmission media. Bit Error Rate (BER), jitter, eye pattern, ratio of rise time and unit interval are some of the different ways designers use to determine signal quality. In this article, eye patterns will be used to demonstrate signal quality for LVDS driver and receiver.

In order to create an eye pattern, a PRBS (Pseudo Random Bit Sequence) of 511 ($2^9 - 1$) bits NRZ data was used to drive the LVDS driver inputs. The LVDS driver was connected to a LVDS receiver with a 10m, 25 pair, 28AWG, twp cable (SCSI grade cable). The eye was plotted on the differential driver output at 155.5 Mbps and also at the receiver input at the end of the cable (see *Figure 8* and *Figure 9*).

A random data pattern is more prone to Inter Symbol Interference (ISI). There is a greater chance of errors occurring from inter symbol interference as the duration of pulses get shorter and shorter. A bit arriving at the receiver input might not have enough time to cross the threshold before the arrival of the next bit, resulting in lost data.

A PRBS with a pattern depth of 511 bits or 2047 ($2^{11} - 1$) or 32767 ($2^{15} - 1$) was used to generate the eye pattern. The eye pattern is then used to characterize inter symbol interference issues. The opening of the eye determines the signal quality, and jitter can be measured at the crossing point. Other industry standards, SONET/SDH for example, specifies eye patterns for signal quality analysis. LVDS technology demonstrates a wide eye opening at 155.5 Mbps over the 10m twp cable. Also refer to application note AN-808 "Long Transmission Line and Data Signal Quality" for more discussions on signal quality.

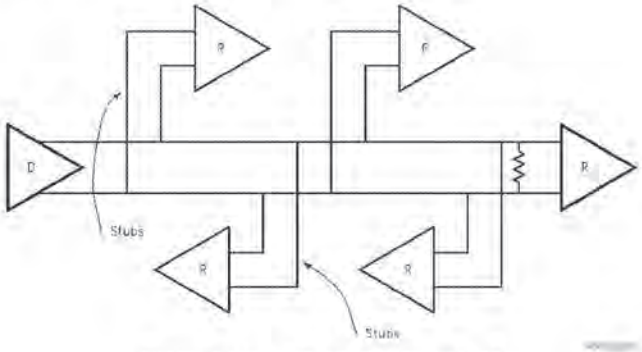

FIGURE 7. Multi-Drop Configuration for LVDS

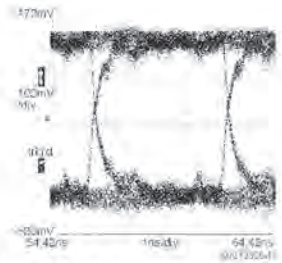

FIGURE 8. Eye Pattern at Driver Output

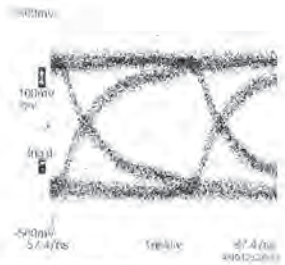

FIGURE 9. Eye Pattern at Receiver Inputs with 10m Cable

CONCLUSION

LVDS technology solves the ever increasing data rate problem while decreasing power dissipation and can be widely used in Telecom, Routers, Intelligent Hubs, LCD displays, Copiers and numerous other exciting applications. LVDS technology provides the best solution for power budget requirements in today's designs. This high speed interface allows designers to implement a simple point-to-point link without complex termination issues. Low power dissipation and the use of a core process allows for the integration of PLLs and digital blocks to provide optimized interface single chip solutions. LVDS technology provides solutions when Megabits at milliwatts are required.

REFERENCES

For TIA standards contact:

Global Engineering Documents

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APPENDIX G

PERICOM®

Application Note 41

A Closer Look at LVDS Technology

By Jimmy Ma

Introduction

With the increase in demand for high throughputs, current technologies are becoming less efficient. Data transmission devices like RS-422, RS-485, SCSI and other devices are limited in data rate and power dissipation. With LVDS, data rate has increased tremendously to meet the demand in the high bandwidth market and yet still consumes less power than many current devices. LVDS offers low-power, low-noise coupling, low EMI emissions, and switching capability beyond many current standards. LVDS applications can be used anywhere where high data rate is required and needed to be transfer over a distance. LVDS technology can be found in printers, flat panels, switches, routers, audio/video digital signal processing and many more other applications. In this application note, it will provide a general overview of LVDS technology.

What is LVDS?

LVDS stands for Low Voltage Differential Signaling. LVDS is defined in the TIA/EIA-644 standards and the IEEE 1596.3 standards. The TIA/EIA-644 standards specified the driver's output and the receiver's input, while the IEEE 1596.3 standards defined the signaling level of LVDS. LVDS features low voltage swing with differential constant current source scheme capable of reaching a maximum recommended data rate of 655Mbps. The theoretical values can reach a maximum rate of 1.923Gbps. It should be noted that the maximum data rate is application specific as well as device specific. LVDS technology can be used with distance ranging from a few inches to 10 meters. Again, noted that the operating distance is also applications and device specific. Standard LVDS are primary designed for point-to-point applications where as, Bus LVDS (BLVDS) was defined to support multi-point applications. Figure 1 shows a generic LVDS point-to-point configuration.

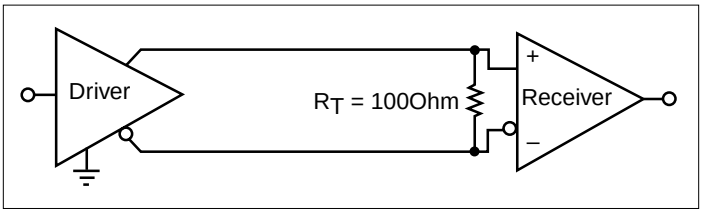

Figure 1. LVDS Circuit

Low Voltage

LVDS voltage swing is the lowest compare RS-422, RS-485, SCSI or any other current devices by today's standards. LVDS voltage swing range from 250mV(minimum) to 450mV (maximum) with a typical value of 350mV. Because the voltage swing is very low and will require less time to rise and fall, it is able to achieve higher operating frequency than CMOS and TTL with the same slew rate. It has an offset voltage of 1.2V above ground. Because its operating voltage is centered around 1.2V with respect to the driver's ground, LVDS does not depend on a specific power supply such as 5V or 3.3V making it easy for LVDS to migrate to new low supply voltage technology. Since it is centered around 1.2V, it is also less susceptible to noise since noise often occurs at Vcc or Ground. Low power consumption and lower current is also another result from the low voltage swing. EMI levels are much less than traditional CMOS, TTL, or even PECL. The low EMI emissions are also due to the use of differential transmission.

Differential Signaling

The communication between the driver and the receiver are done through differential signaling. Differential signaling offers enormous advantages over single-ended technologies because it is less susceptible to noise. In using differential signaling, two-balanced signals are transmitted through the line in opposite direction. Because the signals are of the same magnitude but with opposite direction, the electromagnetic field from the two signals are radiated in opposite direction. As a result, they cancel out most of each other EMI. Figure 2 shows the EMI cancellation effect. Figure 2a, shows a single-ended signal with EMI radiating in only one direction. Figure2b shows a differential signal, with EMI radiating in opposite direction thereby canceling out most of the EMI.

Differential signaling also offers what is known as common-mode rejection at the LVDS receiver's end, which works similar to the EMI canceling effect. The advantage of common-mode rejection is that the receiver will ignore any noise that is coupled equally on the differential signals and only consider the differences between the two signals. Unlike single-ended signal where common-mode rejections are not found, noise on the line may cause the device to trigger unintentionally. Figure 3a shows a single-ended signal. Figure 3b shows a differential signal with common mode rejection. In Figure 3b, the receiver will only consider the 350mV swing differences.

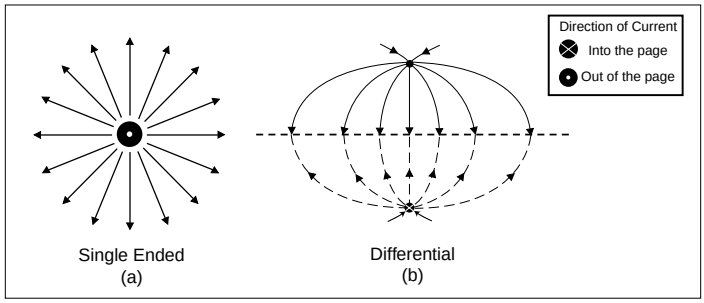

Figure 2. EMI for Single-ended signal and Differential Signal

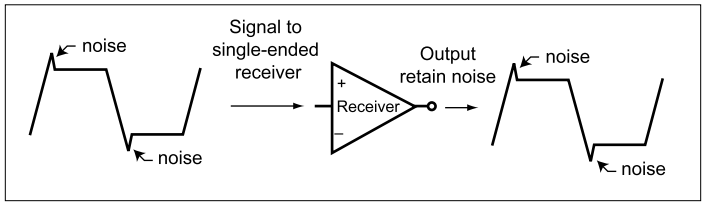

Figure 3a. Noisy input signal to a signal-ended receiver will not eliminate the noise

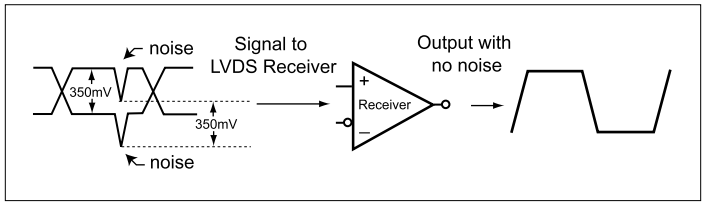

Figure 3b. Differential signals with common-mode rejection at the LVDS receiver. The receiver will only consider the difference between the two signals.

Failsafe

LVDS technology also incorporates a failsafe feature at the receiver's end to force a logic HIGH in an event that an undetermined logic state occurs. The failsafe features are enabled under three conditions: open circuit, short circuit, and terminate circuit. Open condition occurs when the input pins at the receiver's end, that are not in use, are left floating. In an open condition, the output would be forced to a logic HIGH. Without the failsafe feature, pins that are left floating will be able to pick up noise thereby possible giving fault data. For shorted condition, failsafe would also forced a logic HIGH at the output. For terminated condition, if the drive is powered off or is removed from the line, it would also force a logic HIGH at the output. Figure 4a, 4b, and 4c illustrate the three conditions the failsafe features would be enabled.

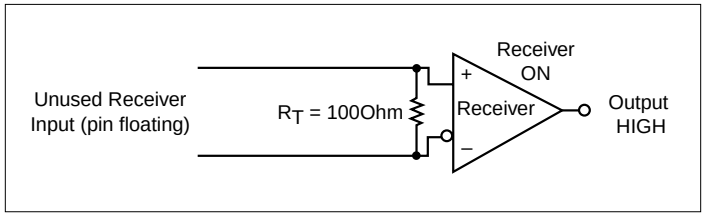

Figure 4a. Failsafe Open Condition

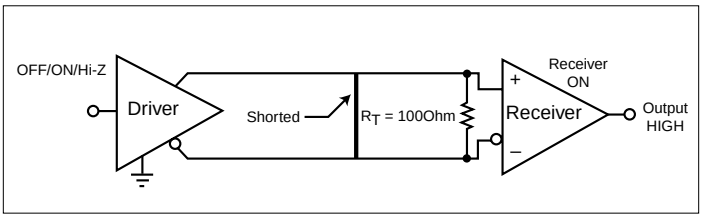

Figure 4b. Failsafe Shorted Condition

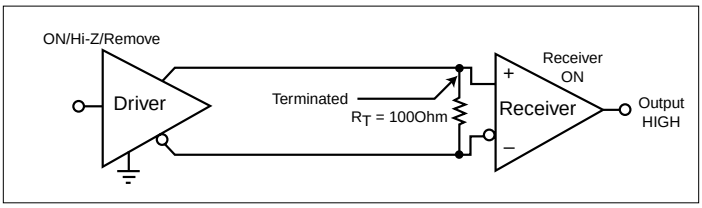

Figure 4c. Failsafe Terminated Condition

Termination

LVDS requires a termination resistor in order to generated a Differential Output Voltage (V_{OD}) across the resistive termination load at the receiver's input. A termination resistor is also required because a current loop of 2.5mA to 4.5mA is needed. LVDS technology operates at sub-nanoseconds level so proper termination is required to obtain good signal qualities and retained minimal reflections. The termination resistor is required because at such high bandwidth, LVDS transmission media such as cable or PCB trace can no longer be treated a simple wire or trace, but as a transmission-line media. An important factor associated with transmission line is that it must be terminated and the termination must matched the characteristic impedance of the PCB trace to prevent reflections from occurring. The characteristic impedance should be matched with a termination resistor of approximately 100Ω and should be placed as close as possible to the input of the receiver. With proper termination, not only reflections are minimal, but also electromagnetic emissions can be reduced. Some LVDS products have embedded termination resistors. It should be noted that proper termination is mandatory for good signal quality, but trace length should also be minimal and have equivalent length to have optimal signal quality.

LVDS vs. PECL

How does LVDS compare to PECL? LVDS and PECL are both capable of high data rate. But with PECL, the power consumption is much greater compared to LVDS. PECL can have as much as 90% more power consumption than LVDS. LVDS is also capable of operating at a low voltage swing of only ±350mV where as PECL has a voltage swing of ±800mV. Figure 4 compares the voltage swing signals between LVDS and PECL. LVDS also benefits over PECL because it does not depend on a specific power supply such as 5V or 3.3V making it easy to migrate to new low power supply technologies than PECL. LVDS technology also has a more simplified termination layout compared to PECL. LVDS requires only one 100Ω termination resistor place at the input of the receiver. Unlike LVDS, PECL requires a more complex termination scheme. Two 220Ω pull-down resistors

are required at the output of the driver as well a 100Ω resistor at the input of the receiver. Figure 6 shows the termination scheme comparison between LVDS and PECL. Table 1 shows a comparison with LVDS and PECL as well as other standards.

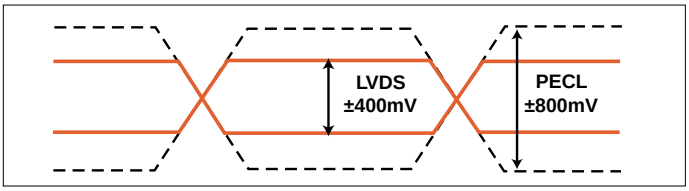

***Figure 5.* PECL and LVDS Voltage Swing Comparision**

Conclusion

LVDS technology is currently one of the fastest low power data transmission available. As the demand for higher data rate increases, LVDS will becomes more crucial. LVDS will become more vital to the solution of new technology such as Hyper Transport whose core technology is based on LVDS technology. Pericom Semiconductor offers a variety of LVDS products, including BUS LVDS and LVDS products with embedded termination resistor.

Parameter	TTL/CMOS	GTL/BTL	RS-422	PECL	LVDS
Signalling	Single Ended	Single \Ended	Differential	Differential Single Ended	Differential
Output Voltage Swing	2.4V - 5.5V	2.4V - 5.5V	±2V	±800mV	±350mV
Reciever Threshold	1.2V - 1.5V	1.2V	±200mV	±200mV	±100mV
Maximum Speed	<100Mbps	<100Mbps	>10Mbps	>400Mbps	>400Mbps
Drive Current	75mA	40mA-80-mA	150mA	40mA-60m-A	3mA-10-mA
Noise generation	High	Medium	Low	Medium	Low
Power Dissipation	High	Medium - High	Low	Medium	Very Low

Table 1. Comparison between LVDS and Other Standards

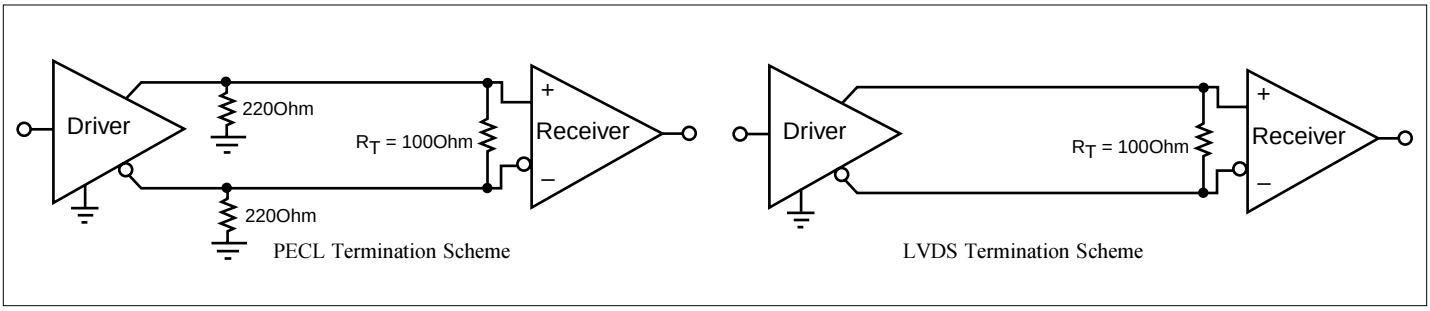

Figure 6. Termination Scheme for PECL and LVDS

LVDS Advantages

- high data rate (1.923Gbps maximum)
- does not depend on a specific power supply
- low power
- low cost
- low EMI (noise)

Glossary

LVDS – Low Voltage Differential Signaling

RS-422 – EIA serial transmission standard that extends transmission speeds and distances beyond those of RS-232, RS-423 is an unbalanced system; RS-422 is a balanced system with a higher level of \ noise immunity. (RS-422)-Electrical characteristics of balanced-voltage digital interface circuits.

RS-423 – Electrical characteristics of unbalanced-voltage for digital interface circuits

RS-485 – EIA serial interface standard for multi-point lines

PECL – Positive Emitter Couple Logic

SCSI – Small Computer System Interface
A peripheral I/O interface with a standard independent protocol that allows many different peripheral devices to be attached to the host's SCSI port

EMI – Electromagnetic Interference

IEEE – Institute of Electrical and Electronics Engineering

TIA/EIA-644 – Telecommunications Industry Association/Electronic Industries Association

Reference:

1. TIA/EIA-644 Standards
2. IEEE 1596.3 Standards
3. Stephen Kempainen and John Goldie "Low-Voltage Signaling Yields Megatransfers Per Second with Milliwatts of Power", EDN Sept. 1996